1.1 GENERAL

Toshiba Personal Computer T1200 (hereinafter referred to as T1200) is a portable personal computer which is compatible with IBM PC situated at higher rank of portable computer than Toshiba T1100 PLUS. It provides many powerful functions in spite of its compact size and internal battery pack which is removal. Hardware of the T1200, most of IC chips are C-MOS type so that the power consumption is very little and Gate Array chips are applied so that it is very compact and light weight.

The T1200 is composed of as follows:

System PCB (Printed curcuit board)
3.5-inch floppy disk drive
3.5-inch hard disk drive
LCD (Liquid crystal display)
Keyboard
Intelligent power supply PCB
Built-in modem

FIGURE 1-1 T1200 Personal Computer

A 3.5-inch Floppy disk drive (FDD) is double-sided, double-density, double-track with storage capacity of 720 kilobytes (formatted). A 3.5-inch hard disk drive (HDD) with storage capacity of 20 megabytes is an equipment of the former. The high-resolution liquid crystal display (LCD) with pixels of 640 in columns and 200 in rows.
The keyboard has 82 keys. For most applications it can be used exactly like a standard typewriter keyboard.
Intelligent power supply apart from those ordinary power serving functions, this unit contains a so-called "one-chip microcomputer", and it controls the whole system PCB, FDD, HDD and HDC.
The built-in modem expands the capabilities of your system. The built-in modem enables the system to communicate with an asynchronous communications device through a telephone line. The modem can operate communications at either low (300 bps) or high (1200 bps) speed.

The T1200 provided connecting to the optional devices at the rear panel of the system. There are six connectors such as a parallel printer, an RGB direct drive CRT display, an external FDD, an external key pad and an RS-232C device.

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU

LANG:TSF
LANG:TISB

1.2 SYSTEM PCB

System PCB is composed of the following devices:

- Central processor: CPU (80C86-2) (9.54 MHz/4.77 MHz)
- Numeric data processor: NPU (8087, optional)
- Memory

System memory	...	640	kbytes
Expanded memory	...	384	kbytes
BIOS ROM	...	32	kbytes
Video RAM	...	16	kbytes

- System support elements
    - Direct memory access: DMA (82C37)
    - Timer : (82C53)
    - Programmable interrupt controller: PIC (82C59)
- Floppy disk controller: FDC (8565)
- Keyboard controller: KBC (80C49)
- Acynchronous communication element: ACE (8570)
- Gate array
    - Bus driver
    - Bus controller
    - EXP-MEM controller
    - Display controller

1.2.1 Jumper straps

The system PCB has five jumper straps; PJ17, PJ18, PJ19, PJ20, and PJ21.

The following figure shows location of the jumper straps.

FIGURE 1-2 Jumper Straps Location

The following table shows function of the jumper straps.

TABLE 1-1 Jumper Strap Functions

Jumper	Pins	Description

```
  ³        ³ ÚÄÄÄÄÄÄÄÄ¿        ³
³
  ³        ³ ³ 1   2 ³         ³    F/F type
³
  ³ PJ17  ³ ÀÄÄÄÄÄÄÄÄÙ        ³
³
  ³        ³   1   2           ³    F/H type
³

ÃÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄ´
  ³        ³   PJ18            ³
³
  ³        ³ ÚÄÄÄÄÄÄÄÄ¿        ³
³
  ³        ³ ³ 1   2 ³ 3       ³    Normal
³
  ³ PJ18  ³ ÀÄÄÄÄÄÄÄÄÙ        ³
³
  ³ PJ19  ³  PJ19 1   2       ³
³
  ³
ÃÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
  ³        ³  PJ18             ³
³
  ³        ³       ÚÄÄÄÄÄÄÄÄ¿  ³    When connect an ICE to the   co-
processor  socket.³
  ³        ³     1 ³ 2   3 ³   ³
³
  ³        ³       ÀÄÄÄÄÄÄÄÄÙ  ³
³
  ³        ³       ÚÄÄÄÄÄÄÄÄ¿  ³
³
  ³        ³  PJ19 ³ 1   2 ³   ³
³
  ³        ³       ÀÄÄÄÄÄÄÄÄÙ  ³
³

ÃÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄ´
  ³        ³ ÚÄÄÄÄÄÄÄÄ¿        ³
³
  ³        ³ ³ 1   2 ³         ³    No  co-processor.
³
  ³ PJ20  ³ ÀÄÄÄÄÄÄÄÄÙ        ³
³
  ³        ³   1   2           ³    When connect a   co-processor to the
³
  ³        ³                   ³     co-processor socket.
³

ÃÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄ´
  ³        ³ ÚÄÄÄÄÄÄÄÄ¿        ³
³
  ³        ³ ³ 1   2 ³         ³    Display a normal font.
³
  ³        ³ ÀÄÄÄÄÄÄÄÄÙ        ³
³
```

PJ21	1 2	Displays a North Europian (Denmark) font.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

1.3 3.5-INCH FLOPPY DISK DRIVE

The floppy disk drive (FDD) used in the T1200 is high performance, high reliable, slim sized FDD for 3.5-inch floppy disks with recording capacity of 1 Mbyte (unformatted) in double-sided, double density and 135 tracks per inch operation. The specifications are as following table.

FIGURE 1-3 3.5-inch FDD

TABLE 1-2 3.5-inch Floppy Disk Drive Specifications

Item	Specifications
Storage Capacity (kilobytes)	1000 (unformatted) 720 (formatted)
Number of Heads	2
Number of Track per Side	80
Track to Track Access (milliseconds)	6
Head Settling Time (milliseconds)	15
Track Density (tracks per second)	135
Motor Start-up Time (milliseconds)	500
Data Transfer Rate (kilobits per second)	250
Rotational Speed (revolutions per minute)	300

Recording Method	MFM (Modified frequency modulation)

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

1.4 HARD DISK DRIVE

The hard disk drive (HDD) is random access storage, having recording capacity of 20 Mbytes. This is equipped with the storage media of non-removable 3.5-inch magnetic disks and mini- winchester type magnetic heads.
The specifications are as following table.

FIGURE 1-4 3.5-inch Hard Disk Drive

TABLE 1-3 3.5-inch Hard Disk Drive Specifications

Item	Specifications
Storage Capacity (megabytes)	25.3 (unformatted) 21.4 (formatted)
Number of Heads	2
Number of Track per Side	615
Access Time (milliseconds) (minimum)	24
(average)	78

(maximum)	130
Data Transfer Rate (megabits per second)	7.5
Rotational Speed (revolutions per minute)	2597
Recording Method	2-7 RLL (Run Length Limited)

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

1.5 HARD DISK CONTROL PCB

Hard disk control PCB (HDC) is accompanied by hard disk drive (HDD) and connects to the system PCB through a cable. This HDC can interface the HDD to the system PCB.

The specifications are as following table.

FIGURE 1-5 Hard Disk Control PCB

TABLE 1-4 Hard Disk Control PCB Specifications

Item	Specifications
Encoding method	2-7 RLL (Run Length Limited)

```
 ³ Data Transfer Rate (megabits per second)   maximum³                  7.5
³

ÃÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄÄÄÄ´
 ³ Write Precompensation time (nanoseconds)        ³                 12
³

ÃÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄÄÄÄ´
 ³ Sectoring                                      ³
Soft         ³

ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÁÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÙ
```

1.6 KEYBOARD

The keyboard is mounted on the system and has 82 keys. These consist of 48 standard keys, 10 function keys, 10 cursor keys, 13 functional keypads, and Fn key.
The keyboard is just a key matrix built up by the above keys. The keyboard is connected to the keyboard controller on the system PCB through a 22-pin flat cable.

FIGURE 1-6 Keyboard

LANG:TISB

1.7 LIQUID CRYSTAL DISPLAY

The liquid crystal display (LCD) is a graphics type display unit which has a resolution of 640 in horizontal (or column) by 200 in vertical (or row) directions. This unit is composed of the display panel, power supply and driver circuits. This receives timing pulses, four-bit data signals, +5V dc and -22V dc power inputs and a contrast control input from the system PCB. All timing pulses and data signals are TTL level compatible. Specifications are as following table.

FIGURE 1-7 Liquid Crystal Display

TABLE 1-5 Liquid Crystal Display Specifications

Item	Specification
Outline Dimension (mm)	275.0 (W) x 126.0 (H) x 15.8 (D)
Number of Dots	640 x 200 dots
Number of characters	80 x 25 (2000) Characters (8 x 8 dot format, alpha-numeric)
Clear Viewing Area (mm)	231.0(W) x 105.0(H)
Dot Size (mm)	0.32 (W), 0.46 (H)
Dot Pitch (mm)	0.35 (W), 0.49 (H)
Weight (gram)	Max. 500

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

1.8 POWER SUPPLY PCB

The power supply PCB supplies dc 5, 12, -22, and -9 volts to all the components in the system.
It is an intelligent power supply using a 1-chip micro-computer and it contains the following functions.

Control and monitoring of the stored main battery. This performs recharge control, detection of the available capacity, and that of the low battery.

1. Monitoring of AC adapter
2. Monitoring of DC output voltage
3. Power on/off control of the system unit
4. Self-diagnosis of the power supply
5. Pays a role of interface with the CPU
    - Communication control
    - Reset signal generation
    - Low-battery signal generation
6. Display control
    - AC adapter connection
    - Battery recharge
    - Abnormal power supply

Output rating is as following table.

FIGURE 1-8 Power Supply PCB

TABLE 1-6 Power Supply PCB Output Rating

FUNCTION	DC VOLTAGE	REGULATION TOLERANCE (%)	MAX. CURRENT
SYSTEM LOGIC, FDD MOTOR	5	5	0.7 A
HDC, HDD (LOGIC)	5	5	0.3A
HDD (MOTOR)	5	10	1.3A
CMOS, DRAM, V-RAM, B-RAM	5	5	80 mA
RS-232C, I/O SLOT	12	5	30 mA

HDD	12	5	10mA
LCD	-22	5	10mA
RS-232C, BUILT IN MODEM OR I/O SLOT	-9	15	30mA

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

1.9 BUILT-IN MODEM

The built-in modem is connected to the connector that is used exclusively for this system PCB. Note that the system PCB is originally provided with this modem. This modem can operate in only one communication mode; the BELL 103/212 communication. The specifications are as following table.

FIGURE 1-9 Built-in Modem

TABLE 1-7 Built-in Modem Specifications

Item	Specification
Data format	
Low Speed (300 BPS)	7 or 8 bits, 1 or 2 stop bits odd, even or no parity.
High Speed (1200 BPS)	7 bits, no parity, 2 stop bits 7 bits, e/o parity, 1 stop bit 8 bits, no parity, 1 stop bit
Dialing Capability	Tone Dial/Pulse Dial
Audio Monitor	Speaker

Receive Sensitivity	-45 dBm

1.9.1 Jumper straps

The built-in modem has four jumper straps; PJ3, PJ4, PJ5 and PJ6.

The following table shows functions of the jumper straps.

TABLE 1-8 Jumper Straps Functions

Jumper Strap Functions

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

2.1 GENERAL

These problem isolation procedures are used to isolate defective FRUs (field replaceable units) to be replaced. FRUs consist of the following:

1. Power supply PCB
2. System PCB
3. FDD
4. HDD and HDC
5. Keyboard
6. LCD

See PART 4 for detailed replacement procedures instructions. Test program operations are described in PART 3.

The following items are necessary for carrying out the problem isolation procedures.

1. T1200 Diagnostics disk
2. Flatbladed screwdriver
3. Work disk (for FDD testing)
4. Cleaning disk kit (for FDD testing)
5. Multimeter
6. Printer port LED

The problem isolation flowchart described in part 2.2 can be used to determine the necessary isolation procedures to be followed when there is a problem with the T1200.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

2.2 PROBLEM ISOLATION FLOWCHART

This flowchart is used as a guide for determining which FRU is defective. Please confirm the following before performing the flowchart procedures.

1. No disk is in the FDD.
2. The HDD switch is off.
3. The ac adapter is disconnected.
4. All optional equipment is disconnected.

See next page.

FIGURE 2-1 Problem Isolation Flowchart

FIGURE 2-1 Problem Isolation Flowchart   con't.

1. If an error is generated on the system test, memory test, display test and real time test, go to system PCB isolation procedures in part 2.4.

2. If an error is generated on the keyboard test, go to keyboard isolation procedures in part 2.8.

3. If an error is generated on the floppy disk test, go to FDD isolation procedures in part 2.5.

MODEL:T1200F/FB

LANG:TAIS

LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

2.3 POWER SUPPLY PCB ISOLATION PROCEDURES

This section describes how to determine whether the power supply PCB is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Battery Check

PROCEDURE 2: Power Supply Indicator Check

PROCEDURE 3: Connector Check

PROCEDURE 4: Output Voltage Check

PROCEDURE 5: Power Supply PCB Replacement

PROCEDURE 1

Battery Check

1. Turn the POWER switch off.

2. Disconnect the ac adapter.

3. Turn the POWER switch on. If the Low Battery indicator lights, plug the ac adapter into the DC IN 12V jack. If the indicator then goes out, the battery is normal and you should go to PROCEDURE 3; if it remains lit, go to PROCEDURE 2.

FIGURE 2-2 Battery Check

PROCEDURE 2

Power Supply Indicator Check

1. Turn the POWER switch on.

2. Plug the ac adapter into an electrical outlet and the DC IN 12V jack.

3. If the Power Supply indicator lights, its meaning depends on its color and whether it blinks or not, as described below.

   RED/CONTINUOUSLY LIT: Current is flowing; the ac adapter is normal.

GREEN/CONTINUOUSLY LIT: Either the main battery is disconnected, or current flow has stopped (charging is complete); the ac adapter is normal.

RED/BLINKING: Current is not being supplied by the ac adapter; the adapter must be replaced. If the indicator still blinks after replacing the ac adapter, replace the power supply PCB. (See part 4.8)

4. If the indicator does not light the ac adapter must be replaced.

FIGURE 2-3 Power Supply Indicator

PROCEDURE 3

Connector

1. Turn the POWER switch off and disconnect the ac adapter.

2. Remove the top cover assembly. (Refer to part 4.2.)

3. If the three power supply PCB connectors (PJ 2, 3, and 4) and the two system PCB connectors (PJ 9 and 12) are connected properly, go to PROCEDURE 4; if they are not connected properly, reconnect them.

<fig id=MMS\1200\12002_7.TIF>FIGURE 2-4 Power Supply and System PCB Connectors

PROCEDURE 4

Output Voltage Check

1. Turn the POWER switch off.

2. Remove the power supply PCB. (Refer to part 4.8)

3. Plug the ac adapter into an electrical outlet and the DC IN 12V jack.

4. Turn the POWER switch on.

5. Use a multimeter to confirm that the output voltages for the three power supply PCB connectors conform to the values given in the following table.

6. If the voltages conform to the values given in the table, the power supply PCB is normal. System PCB is probably defective, go to system PCB isolation procedures in part 2.4.

7. If the voltages do not conform to those given in the table, go to PROCEDURE 6.

TABLE 2-1 Power Supply PCB Output Voltages

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÂÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÂÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³               ³     PIN NUMBER   ³      VOLTAGE (  Vdc)         ³
```

CONNECTOR	+ lead	-lead	Normal	Min	Max
PJ 2	1	2	+5	+4.75	+5.25
PJ 4	6	3, 7, 10	+5	+4.75	+5.25
	8	3, 7, 10	+12	+11.4	+12.6
	9	3, 7, 10	-9	-10.35	-7.65
	12	3, 7, 10	-22	-23.1	-20.9
PJ 5	1	GND	+5	+4.5	+5.5
	2	GND	+5	+4.75	+5.25
	3	GND	+12	+11.4	+12.6

PROCEDURE 5

Power Supply PCB Replacement

1. Turn the POWER switch off.

2. Disconnect the ac adapter from the DC IN 12V jack.

3. Replace the power supply PCB. (Refer to part 4.8)

4. If normal operation is restored after replacing the PCB, the previous PCB was defective.

5. If normal operation is not restored, another FRU is probably defective. The defective unit must be isolated and replaced.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

2.4 SYSTEM PCB ISOLATION PROCEDURES

This section describes how to determine whether the system PCB is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Message Check

PROCEDURE 2: Printer Port LED Check

PROCEDURE 3: Jumper Straps Check

PROCEDURE 4: Test Program Execution

PROCEDURE 5: System PCB Replacement

NOTE: Before carrying out any of these procedures, make sure that there is not a floppy disk in the FDD and the HDD switch is off.

PROCEDURE 1

Message Check

1. If the following message is displayed on the screen, the system PCB is normal.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ Place system disk in drive                       ³
³ Press any key when ready....                     ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

2. If the above message is not displayed, check to see if any of the following messages are displayed.

TABLE 2-2 Error Messages

KEYBOARD ERROR
FDD ERROR
OPTION ERROR
RTC ERROR
DISK 0 FAILURE
DISK CONTROLLER FAILURE

3. If any of the above messages are displayed, go to PROCEDURE 3.

4. If none of the above messages are displayed, go to PROCEDURE 2.

PROCEDURE 2

Printer Port LED Check

1. Turn the POWER switch off.

2. Plug the printer port LED into the PRT (printer) connector on the back of the unit.

3. Turn the POWER switch on while watching the printer port LED. The printer port LED will light at the same time that the POWER switch is turned on.

4. Read the final LED status as a hexadecimal value from left to right.

5. If the final LED status matches any of the error status and OK status values in the following table, go to PROCEDURE 5.

6. If the final LED status is FEH, go to PROCEDURE 3 and continue.

TABLE 2-3 Printer Port LED Error Status and OK Status

Test Name	Error Status	OK Status
BIOS ROM test	01H	11H
Timer (82C53) test	02H	
	03H	12H
DMAC (82C37) test	04H	
	05H	14H
RAM R/W test (first 16kbytes)	06H	
	07H	16H
PIC (82C59) test	08H	
	09H	
	0AH	
	0BH	1BH
Video RAM test	0CH	
Display controller test	0DH	
	0EH	

PROCEDURE 3

Jumper Strap Check

1. Turn the POWER switch is off.

2. Remove the top cover assembly. (Refer to part 4.2.)

3. Confirm that the jumper straps status is normal. (Refer to part 1.2.1.)

4. If the jumper strap status is normal, go to PROCEDURE 4.

5. If the jumper strap status is not normal, set them correctly.

FIGURE 2-5 Jumper Straps

PROCEDURE 4

Test Program Execution

1. Execute the following test program. (See PART 3 TEST AND DIAGNOSTICS.)

    1. System test
    2. Memory test
    3. Keyboard test
    4. Display test
    5. Floppy disk test
    6. Real time test

2. If an error is generated on the system test, memory test, display test and real time test, go to system PCB isolation procedures in part 2.4.

3. If an error is generated on the floppy disk test, go to FDD isolation procedures in part 2.5.

4. If an error is generated on the keyboard test, go to keyboard isolation procedures in part 2.7.

PROCEDURE 5

System PCB Replacement

1. Replace the system PCB. (Refer to part 4.13)

2. If normal operation is restored after replacing the PCB, the previous PCB was defective.

3. If normal operation is not restored, another FRU is probably defective. The defective unit must be isolated and replaced.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

2.5 FLOPPY DISK DRIVE ISOLATION PROCEDURES

This section describes how to determine whether the floppy disk drive is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Test and Diagnostic Program Loading Check

PROCEDURE 2: Message Check

PROCEDURE 3: Head Cleaning

PROCEDURE 4: FDD Test Execution

PROCEDURE 5: FDD Connector Check

PROCEDURE 6: New FDD connection

NOTE: Make sure that the HDD switch is off.

PROCEDURE 1

Test and Diagnostic Programs Loading Check

1. Turn the POWER switch off.

2. Insert the diagnostics disk into the FDD.

3. Turn the POWER switch on.

4. If loading occurs normally, go to PROCEDURE 3. (See PART 3 to determine if loading has occurred normally.)

5. If loading has not occurred normally, go to PROCEDURE 2.

PROCEDURE 2

Message Check

1. When the diagnostics disk is inserted into the FDD and the POWER switch is turned on, either message (a) or message (b) should appear.

```
   ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
(a)³ Place system disk in drive                            ³
   ³ Press any key when ready....                          ³
   ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ

   ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
(b)³ Non-System disk or disk error                         ³
   ³ Replace and press any key when ready                  ³
   ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

2. If either of the above messages is displayed, the contents of the floppy disk are damaged, or some other disk than the diagnostics disk has been inserted into the FDD. Change the diagnostics disk. If loading then occurs, go to PROCEDURE 4; if loading does not occur, go to PROCEDURE 3.

3. If neither of the above messages appears, go to PROCEDURE 5.

PROCEDURE 3

Head Cleaning

1. Turn the POWER switch off.

2. Insert the cleaning disk to the FDD.

3. Turn the POWER switch on, then will clean the head of the FDD.

4. Remove the cleaning disk from the FDD.

5. If normal operation is restored after cleaning the head, go to PROCEDURE 4.

6. If normal operation is not restored, go to PROCEDURE 5.

PROCEDURE 4

FDD Test Execution

1. Run the floppy disk test which is indicated in the Diagnostic Test Menu.

2. If an error is generated during the floppy disk test, an error code and status will be displayed as indicated in the following table. Follow the directions provided in the table.

3. If no error is generated, the FDD is normal.

TABLE 2-4 FDD Error Statuses

CODE	STATUS
01	Bad Command
02	Address Mark Not Found
03	Write Protected
04	Record Not Found
06	Media removed on dual attach card
08	DMA Overrun Error
09	DMA Boundary Error
10	CRC Error
20	FDC Error
40	SEEK ERROR
60	FDD not drive
80	Time Out Error (Not Ready)

EE	Write buffer error

PROCEDURE 5

FDD Connector Check

1. Turn the POWER switch off and disconnect the ac adapter from the DC IN 12V jack.

2. Remove the top cover assembly. (Refer to part 4.2.)

3. If the FDD cable is connected to the system PCB securely, and if the A and B drives are connected correctly, go to PROCEDURE 6.

4. If the above connections are not secure, reconnect them.

FIGURE 2-6 FDD Connector Check

PROCEDURE 6

New FDD Connection

1. Turn the POWER switch off.

2. Remove the FDD. (Refer to part 4.10.)

3. Connect the new FDD to the FDD connector, then other connectors too.

4. Turn the POWER switch on.

5. If normal operation is restored after connect the new FDD, the previous FDD was defective. Assemble the system.

6. If normal operation is not restored, system PCB is probably defective. Refer to part 2.4.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

2.6 HARD DISK DRIVE ISOLATION PROCEDURES

This section describes how to determine whether the Hard Disk Drive is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: HDD Indicator Check

PROCEDURE 2: Format Execution

PROCEDURE 3: Hard Disk Test Execution

PROCEDURE 4: Connector Check

PROCEDURE 5: Jumper Strap Check

PROCEDURE 6: New HDD Connection

Note: Make sure that the HDD switch is on.

PROCEDURE 1

HDD Indicator Check

1. Turn the POWER switch off.

2. If there is a floppy disk in the FDD, take it out.

3. Confirm that the HDD switch turn on, then turn the POWER switch on.

4. If the HDD indicator (C Lower) blinks briefly and goes out, go to PROCEDURE 2; if it continues blinking, go to PROCEDURE 2.

5. If the indicator does not light at all, go to PROCEDURE 4.

FIGURE 2-7 HDD Indicator Check

PROCEDURE 2

Format Execution

CAUTION: The contents of the hard disk will be erased when the FORMAT command is run. Before running the test, transfer the contents of the hard disk on the floppy disk. This can be done with the MS-DOS BACKUP command. (See the MS-DOS manual for details.)

1. Remove the diagnostics disk, and then insert the MS-DOS system disk to the FDD.

2. To set the partition of the hard disk, enter the FDISK command. (See the MS-DOS manual for details.)

3. To format the hard disk, enter the FORMAT command. (See the MS-DOS manual for details.)

4. If normal operation is restored, the HDD is normal.

5. If normal operation is not restored, go to PROCEDURE 6.

PROCEDURE 3

Hard Disk Drive Test Execution

CAUTION: The contents of the hard disk will be erased when the test program is run. Before running the test, transfer the contents of the hard disk on the floppy disk. This can be done with the MS-DOS BACKUP command. (See the MS-DOS manual for details.)

1. Insert the diagnostics disk into the FDD and load the test and diagnostic programs.

2. Run the hard disk test which is indicated in the diagnostics test menu.

3. If an error is generated during the hard disk test, an error code and status will be displayed as indicated in the following table. Go to PROCEDURE 3.

4. If no error is generated, the HDD is normal. Enter the MS-DOS FDISK command which will set the partition. Then enter the MS-DOS FORMAT command. (See the MS-DOS manual for details.)

TABLE 2-5 HDD Error Statuses

CODE	STATUS
01	Bad command error
02	Bad address mark
04	Record not found
05	HDC NOT RESET
07	Drive not initialize
09	DMA Boundary error
0A	Bad sector error
0B	Bad track error
10	ECC error
11	ECC recover enable
20	HDC error
40	Seek error
80	Time out error

AA	Drive not ready
BB	Undefined
CC	Write fault
E0	Status error
F0	Not sense error (HW.code = FF)

PROCEDURE 4

Connector Check

1. Turn the POWER switch off.

2. Disconnect the ac adapter from the DC IN 12V jack.

3. Remove the top cover assembly. (Refer to part 4.2)

4. If the HDD, HDC, and system PCB are connected securely, go to PROCEDURE 5.

5. If they are not connected securely, reconnect them.

FIGURE 2-8 HDC and HDD Connector Check

PROCEDURE 5

Jumper Strap Check

1. Confirm that a jumper strap (PJ 17) on the system PCB and a jumper strap (PJ 9) on the hard disk control PCB is as following status. (Refer to part 1.2.1 and 1.5.1.)

   PJ 17 (system PCB)................. Open
   PJ 9 (hard disk control PCB)....... Short

2. If the jumper strap is above status, go to PROCEDURE 6.

3. If the jumper strap is not above status, set the jumper strap correctly.

Hard Disk Control PCB

System PCB

FIGURE 2-9 Jumper Straps

PROCEDURE 6

New HDC Connection

1. Turn the POWER switch off and disconnect the ac adapter from the DC IN 12V jack.

2. Replace the HDC. (Refer to part 4.11.)

3. Connect the new HDC to the system PCB and HDD, then other connectors too.

4. If normal operation is restored, the previous HDC was defective. Assemble the system.

5. If normal operation is not restored, HDD is probably defective. Go to PROCEDURE 7.

PROCEDURE 7

New HDD Connection

1. Turn the POWER switch off.

2. Remove the HDD. (Refer to part 4.12.)

3. Connect the new HDD to the HDC, then other connectors too.

4. If normal operation is restored, the previous HDD was defective. Assemble the system.

5. If normal operation is not restored, system PCB is probably defective. System PCB is probably defective. Refer to part 2.4.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

2.7 KEYBOARD ISOLATION PROCEDURES

This section describes how to determine whether the keyboard is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Input Check

PROCEDURE 2: Keyboard Test Execution

PROCEDURE 3: Connector Check

PROCEDURE 4: New Keyboard Connection

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PROCEDURE 1

Input Check

1. Load either the diagnostics disk or the MS-DOS system disk.

2. When a prompt (A, B, C, etc.) appears on the screen, hit any of the white keys on the keyboard (any character or the space bar). If the character you hit appears on the screen, go to PROCEDURE 2.

3. If the character does not appear, go to PROCEDURE 3.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ Toshiba Personal Computer MS-DOS Version 3.20/(RXXXXXX) ³
³                                                          ³
³      (C) Copyright Toshiba Corporation 1983,1986        ³
³                                                          ³
³      (C) Copyright Microsoft Corporation 1981,1986      ³
³                                                          ³
³ Current date is XXX X-XX-19XX                           ³
³ Enter new date ( mm-dd-yy):___                           ³
³ Current time is X:XX:XX,XX                              ³
³ Enter new time:___                                      ³
³                                                          ³
³ COMMAND Version 3.20                                    ³
³ A>  abcdefghijklmnopqrst...........                      ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

FIGURE 2-10 Keyboard Input Check

Page 2-33

PROCEDURE 2

Keyboard Test Execution

1. Insert the diagnostics disk into the FDD and load the test and diagnostics programs. (Refer to PART 3.)

2. Run the keyboard test which is indicated in the diagnostics test menu.

3. If an error is generated during the test, go to PROCEDURE 3.

4. If no error is generated during the test, the keyboard is normal.

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PROCEDURE 3

Connector Check

1. Turn the POWER switch off and disconnect the ac adapter from the DC IN 12V jack.

2. Remove the top cover assembly. (Refer to part 4.2)

3. Lift the keyboard up and check that the keyboard cable is connected securely to the system PCB. If it is connected securely, go to PROCEDURE 4.

4. If it is not connected securely, reconnect it.

FIGURE 2-11 Keyboard Connector Check

PROCEDURE 4

New Keyboard Connection

1. Turn the POWER switch off and disconnect the ac adapter from the DC IN 12V jack.

2. Remove the keyboard unit. (Refer to part 4.4.)

3. Connect the new keyboard to the system PCB.

4. If normal operation is restored after connect the keyboard, the previous keyboard was defective. Assemble the system.

5. If normal operation is not restored, system PCB is probably defective. Refer to part 2.4.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

2.8 LCD ISOLATION PROCEDURES

This section describes how to determine whether the LCD is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Display Check

PROCEDURE 2: LCD Contrast Check

PROCEDURE 3: Display Test Execution

PROCEDURE 4: System PCB Connector Check

PROCEDURE 5: LCD Module Connector Check

PROCEDURE 6: New LCD Cabe Connection

PROCEDURE 7: New LCD Module Connection

PROCEDURE 1

Display Check

1. Turn the POWER switch off.

2. After turning the POWER switch on again, the following message should appear in the upper left-hand corner of the screen:

```
MEMORY TEST XXXKB
```

3. If the message appears, go to PROCEDURE 3.

4. If the message does not appear, first do the following:

    (a) Confirm that the contrast knob is adjusted correctly.

    (b) Confirm that the display is not on an external CRT. (The CRT indicator lamp will be lit if the display is on an external CRT.)

    After confirming (a) and (b) above, perform steps 1 and 2 again. If the message still fails to appear, go to PROCEDURE 2.

PROCEDURE 2

LCD Contrast Check

1. Turn the contrast knob, then confirm that the screen becomes changed darker or brighter.

2. If the screen is changed darker or brighter, power supply inputs voltage to the LCD module. Go to PROCEDURE 7.

3. If the screen is not changed, go to PROCEDURE 4.

FIGURE 2-12 LCD Contrast Check

PROCEDURE 3

Display Test Execution

1. Insert the diagnostics disk into the FDD and run the test and diagnostics programs.

2. If an error is generated during the display test from the

diagnostics test menu, the system PCB is probably defective. Refer to part 2.4.

3. If no error is generated, the LCD is normal.

PROCEDURE 4

System PCB Connector Check

1. Turn the POWER switch off and disconnect the ac adapter from the DC IN 12V jack.

2. Remove the top cover assembly. (Refer to part 4.2.)

3. Confirm that the LCD cable is connected securely to the system PCB connector (PJ 11).

4. If the cable is connected securely, go to PROCEDURE 5.

5. If it is not connected securely, reconnect it.

FIGURE 2-13 System PCB Connector Check

PROCEDURE 5

LCD Module Connector Check

1. Turn the POWER switch off and disconnect the ac adapter from the DC IN 12V jack.

2. Take out the LCD module (Refer to part 4.15.) and confirm that the LCD cable is connected securely to the module.

3. If the cable is connected securely, go to PROCEDURE 6.

4. If the cable is not connected securely, reconnect it.

FIGURE 2-14 LCD Module Connector Check

PROCEDURE 6

New LCD Cable Connection

1. Connect the new LCD cable to the system PCB and LCD module.

2. If normal operation is restored after replacing the LCD module, the previous LCD cable was defective. Assemble the system.

3. If normal operation is not restored, LCD module is probably defective. Go to PROCEDURE 7.

PROCEDURE 7

LCD Module Connection

1. Connect a new LCD module and LCD cable to the system PCB.

2. If normal operation is restored after replacing the LCD module, the previous LCD module was defective. Assemble the system.

3. If normal operation is not restored, system PCB is probably defective. System PCB is probably defective. Refer to part 2.4.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.1 GENERAL

This part explains test and diagnostic programs. The purpose of the test and diagnostic programs is to check the functions of all hardware modules of the T1200 Personal Computer. There are 17 programs; they are composed of two modules: the service program module (DIAGNOSTICS MENU) and test program module (DIAGNOSTIC TEST MENU).
The service program module is composed of 6 tasks:

1. HARD DISK FORMAT
2. HEAD CLEANING
3. LOG UTILITIES
4. RUNNING TEST
5. FDD UTILITIES
6. SYSTEM CONFIGURATION

The test program module is composed of 11 tests as follows:

1. SYSTEM TEST
2. MEMORY TEST
3. KEYBOARD TEST
4. DISPLAY TEST
5. FLOPPY DISK TEST
6. PRINTER TEST
7. ASYNC TEST
8. HARD DISK TEST
9. REAL TIMER TEST
10. NDP TEST
11. EXPANSION TEST

The following items are necessary for carrying out the test and diagnostic programs.

1. T1200 Diagnostics disk
2. MS-DOS system disk
3. Work disk (formatted)
4. Cleaning disk kit
5. Printer wraparound connector
6. RS232C wraparound connector

The service engineer utilizes these programs to isolate problems by selecting the appropriate program and operation procedures described in the part 3.2 OPERATIONS.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.2 OPERATIONS

1. Insert the diagnostics disk in the floppy disk drive and turn the POWER switch on.

2. Input TESTCE12 for the A> prompt and press Enter.

3. The following display will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³  TOSHIBA personal computer T1200 DIAGNOSTICS     ³
³  Version 1.00 (C) copyright TOSHIBA Corp. 1987   ³
³                                                     ³
³  DIAGNOSTIC MENU                                 ³
³                                                     ³
³       1 - DIAGNOSTIC TEST                        ³
³       2 - HARD DISK FORMAT                       ³
³       3 -                                        ³
³       4 - HEAD CLEANING                          ³
³       5 - LOG UTILITIES                          ³
³       6 - RUNNING TEST                           ³
³       7 - FDD UTILITIES                          ³
³       8 - SYSTEM CONFIGURATION                   ³
³       9 - EXIT TO MS-DOS                         ³
³                                                     ³
³  PRESS [1] - [9] KEY                             ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

Detailed explanations of the service programs and the operations are given in parts 3.16 to 3.21.

4. Press 1 key then Enter. The following display will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³  TOSHIBA personal computer T1200 DIAGNOSTICS      ³
³  version 1.00 (C) copyright TOSHIBA Corp. 1987    ³
³                                                      ³
³  DIAGNOSTIC TEST MENU                             ³
³                                                      ³
³         1 - SYSTEM TEST                           ³
³         2 - MEMORY TEST                           ³
³         3 - KEYBOARD TEST                         ³
³         4 - DISPLAY TEST                          ³
³         5 - FLOPPY DISK TEST                      ³
³         6 - PRINTER TEST                          ³
³         7 - ASYNC TEST                            ³
³         8 - HARD DISK TEST                        ³
³         9 - REAL TIMER TEST                       ³
³        10 - NDP TEST                              ³
³        11 - EXPANSION TEST                        ³
³        88 - FDD & HDD ERROR RETRY COUNT SET       ³
³        99 - EXIT TO DIAGNOSTICS MENU              ³
³                                                      ³
³  PRESS [1] - [9] KEY                              ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

If you want to set the FDD and HDD error retry count, type 88 then press Enter. The following message will appear. If don't the operation, FDD and HDD error retry count is once.

```
FDD & HDD Error retry count?
```

You can set the error retry count of the floppy disk test and hard disk test.

Type 99 then press Enter. Return to the DIAGNOSTICS MENU.

When select the FLOPPY DISK TEST, the following messages will appear.

```
Test drive number select (1:FDD1,2:FDD2,0:FDD1&2)?

Media in drive#1 mode (1:360k,2:360k-1.2M/720k,3:1.2M,4:720k)?
```

When select the HARD DISK TEST, the following message will appear.

```
Test drive number select (1:HDD1,2:HDD2,0:HDD1&2)?
```

5. After pressing the test number (1 to 11) of the DIAGNOSTIC TEST MENU, the following display (sample) will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³   TEST NAME                                XXXXXXX     ³
³                                                          ³
³   SUB TEST      : XX                                  ³
³   PASS COUNT    : XXXXX       ERROR COUNT : XXXXX     ³
³   WRITE DATA    : XX          READ DATA   : XX        ³
```

```
³   ADDRESS       : XXXXX       STATUS      : XXX        ³
³                                                           ³
³   SUB-TEST MENU                                        ³
³                                                           ³
³   01 - ROM CHECKSUM                                    ³
³    :   :                                               ³
³    :   :                                               ³
³   99 - Exit to DIAGNOSTIC TEST MENU                    ³
³                                                           ³
³   SELECT SUB-TEST NUMBER? _                            ³
³   TEST LOOP (1:YES/2:NO)? -                            ³
³   ERRR STOP (1:YES/2:NO)? -                            ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

6. Select the subtest number. Type the subtest number then press the Enter. The following message will appear.
   When select the KEYBOARD TEST, the following message will not appear.

   TEST LOOP (1:YES/2:NO)?

   When select the (YES);
   Each time a test cycle ends, it increments the pass counter by one and repeats the test cycle..
   When select the (NO);
   At the end of a test cycle, it terminates the test execution and exits to the subtest menu.

7. Type the 1 or 2 then press Enter. The following message will appear.

   ERROR STOP (1:YES/2:NO)?

   When select the (YES);
   When an error occurs, it displays the error status and stops the execution of the test program. The operation guide displays on the right side of the display screen.
   When select the (NO);
   When an error occurs, it displays the error status then it increments the error counter by one and goes to the next test.

8. Type the 1 or 2 then press the Enter. The test program will run. Each subtest names described in the part 3.3.

9. When stop the test program, press Ctrl + Break keys then return to the DIAGNOSTICS MENU.

10. When error occurs on the test program, the following message will appear.

```
     ERROR STATUS NAME      [[ HALT OPERATION ]]

                               1: Test End

                               2: Continue

                               3: Retry
```

1: Terminates the test program execution and exits to the subtest menu.
2: Continues the test.
3: Retry the test.

The error code and error status names described in part 3.15.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.3 SUBTEST NAMES

The following table shows subtest name of the test program.

TABLE 3-1 Subtest Names

#	TEST NAME	SUBTEST#	TEST ITEMS
1	SYSTEM	01	ROM checksum
		02	HDDOFF - SW
2	MEMORY	01	RAM constant data
		02	RAM address pattern data
		03	RAM refresh
		04	Expansion bus
		05	Backup RAM
		06	EMS function
3	KEYBOARD	01	Pressed key display
		02	Tenkey pad display
		03	Pressed key code display
4	DISPLAY	01	VRAM read/write
		02	Character attributes
		03	Character set
		04	80*25 Character display
		05	320*200 Graphics display
		06	640*200 Graphics display
		07	Display peg.
		08	"H" pattern display
		09	Social attribute test
5	FDD	01	Sequential read
		02	Sequential read/write
		03	Randam address/data

		04	Write specified address
		05	Read specified address
6	PRINTER	01	Ripple pattern
		02	Function
		03	Wrap around
7	ASYNC	01	Wrap around (channel - 1)
		02	Wrap around (channel - 2)
		03	Point to point (send)
		04	Point to point (receive)
		05	Card modem loopback
		06	Card modem on-line test
		07	Dial tester test
8	HDD	01	Sequential read
		02	Address uniquence
		03	Randam address/data
		04	Cross talk & peek shift
		05	Write/read/compare(CE)
		06	Write specified address
		07	Read specified address
		08	ECC circuit (CE cylinder)
9	REAL TIMER	01	Real time
		02	Real time carry
10	NDP	01	NDP
11	EXPANSION UNIT	01	Box wrap around
		02	Box mono video ram

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.4 SYSTEM TEST

Subtest 01   ROM checksum (Execution time: 1 second)

This test performs the ROM checksum test on the system PCB.
(Test extent : F0000H - FFFFFH 64KB)

Subtest 02 HDD off-SW

Note: Confirm that turn the HDD switch on.

After checking the operation of the HDD switch, confirm that signals are being exchange between the CPU and the PS (Power Supply).

Operation for the test is as follows.

1. After executing the test, the following message will appear.

```
*** HDD off-switch test start ***
```

2. Turn the HDD switch off. The following message will appear.

```
*** HDD off-switch test OK ! ***
```

3. Press Enter, then return to the subtest menu of the system test.

3.5 MEMORY TEST

Subtest 01 RAM constant data (Execution time: 58 seconds)

This test writes constant data to Memory, and then reads and compares them with the original data. The constant data are "FFFFH", "AAAAH", "5555H", "0101H" and "0000H".

Subtest 02 RAM address pattern data (Execution time: 17 seconds)

This test makes the segment address and offset address by XORing, and then writes the address pattern data and reads and compares them with the original data.

Subtest 03 RAM refresh (Execution time: 34 seconds)

This test writes constant data in 256 bytes length to Memory, and then reads and compares it with the original data. The constant data are "AAAAH" and "5555H". A certain interval time will be taken between the write and the read operations.

Subtest 04 Expansion bus (Execution time: 3 seconds)

Note: As this test requires a special tool to be executed, it can not be carried out here.

Subtest 05 Backup RAM (Execution time: 1 second)

This test writes data (FFH, AAH, 55H, 00H) to the memory address (F0000H to F07FFH); then read it the data out and compares it to the original data.

Subtest 06 EMS function (Execution time: 16 seconds; 384 kbytes)

CAUTION: The contents of the EMS (Expanded memory specification) will be erased when this test is run. After the test, enter the MS-DOS SETUP12 command, which to set the EMS space. (See the OWNER'S manual for details).

Run the same test as subtest 05 for the EMS memory (384 kbytes) page frame address (D0000H) and the block select register (03H). This is performed for every 64kbytes. Operations for the test is as follows.

1. After executing the test, the following message will appear.

```
Warning: The contents of the EMS will be destroyed
         Press [Enter] key.
```

2. Press the Enter then the following message will appear.

```
[EMS port = XXXH, BLOCK# = X, PAGE = XXXXX]
```

3. Automatically return to the subtest menu of the MEMORY TEST.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.6 KEYBOARD TEST

Subtest 01   Pressed key display

Note: Execute the test when Num-lock key is off. If this key is on, the test cannot be carried out.

When the keyboard layout (as shown below) is drawn on the display, press a certain key and check whether the corresponding key on the screen is changed to the character "*".
When the same key again, it becomes to be the original state so that it is able to confirm the self-repeat function.
The following three keys are exceptions, and each key is changed to the character "*" only when it is pressed, and if released, it gets back to the original state.

Ctrl key, Shift key, Alt key

```
KEYBOARD TEST IN PROGRESS 30100
```

Subtest 02   Tenkey pad display

Note: This test can be executed only when the Tenkey pad is connected to the key pad connector.

When the keyboard layout is drawn on the display, press a certain key of the tenkey pad, and confirm that the corresponding key on the display is changed to the character "*"
When the same key is pressed again, it gets back to the original stats so that it is able to confirm the self-repeat function.

```
KEYBOARD TEST IN PROGRESS 30200
```

Subtest 03   Pressed key code display

Scan code, character code, and key top name are displayed on the screen by pressing a certain key as shown below.
Some keys such as Ins, Caps lock, Num lock, Scroll lock, Alt, Ctrl, and shift key blink on the screen when each one is pressed.
Each scan code, character code and key top name described in the TABLE 3-2.(Next page)

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³                                                        ³
³ KEYBOARD TEST         IN PROGRESS       303000      ³
³                                                        ³
³     Scan code      =    XX                          ³
³                                                        ³
³     Character code =    XX                          ³
³                                                        ³
³      Keytop         =    XXXX                        ³
³                                                        ³
³ Ins Lock    Caps Lock     Num Lock Scroll Lock       ³
```

```
³                                                        ³
³ Alt         Ctrl        Left Shift     Right Shift ³
³                                                        ³
³ PRESS [ENTER] KEY                                   ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

TABLE 3-2 Scan Code, Character Code, and Key Top Name

KEY TOP	SCAN CODE	CHARACTER CODE
'	29	60
1	02	31
2	03	32
3	04	33
4	05	34
5	06	35
6	07	36
7	08	37
8	09	38
9	0A	39
0	0B	30
-	0C	2D
=	0D	3D
\	2B	5C
	0F	09
q	10	71
w	11	77
e	12	65
r	13	72
t	14	74
y	15	79
u	16	75
i	17	69
o	18	6F

p	19	70
[	1A	5B
]	1B	5D
a	1E	61
s	1F	73
d	20	64
f	21	66
g	22	67
h	23	68
j	24	6A
k	25	B6
l	26	6C
;	27	3B

<fig id=MMS\1200\12003_12.TIF>Page 3-12

TABLE 3-2 Scan Code, Character Code, and Key Top Name

KEY TOP	SCAN CODE	CHARACTER CODE
'	28	27
z	2C	7A
x	2D	78
c	2E	63
v	2F	76
b	30	62
n	31	6E
m	32	6D
,	33	2C
.	34	2E
/	35	2F
Space	39	20

F2	3C	00
F4	3E	00
F6	40	00
F8	42	00
F10	44	00
F1	3B	00
F3	3D	00
F5	3F	00
F7	41	00
F9	43	00
Esc	01	1B
Home	47	00
	4D	00
Pg Dn	51	00
Del	53	00
Sys Req	85	00
Prt Sc	37	2A
-	4A	2D
+	4E	2B

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

<fig id=MMS\1200\12003_13.TIF>Page 3-13

3.7 DISPLAY TEST

Subtest 01   VRAM read/write (Execution time: 1 second)

This test writes constant data (FFFFH, AAAAH, 5555H, 0000H) and address data to the video RAM; it then reads the data out and compares it the original data.

Subtest 02   Character attributes (Execution time: 1 second)

This test is for checking the various types of displays:

Normal Display
Intensified Display
Reverse Display
Blinking Display

In the case of color displays, all seven colors used (blue, red, magenta, green, cyan, yellow, white) are displayed. The background and foreground colors can then be checked for brightness. The display below appears on the screen when this test is run.

CHARACTER ATTRIBUTES

Page 3-14

Subtest 03   Character set (Execution time: 1 second)

In this test the character code (00H to FFH) characters are displayed in the 40 x 25 pixel mode as shown below.

CHARACTER SET IN 40X25

Subtest 04   80*25 Character display (Execution time: 1 second)

In this test the shift characters are displayed in the 80 x 25 pixel mode as shown below.

80*25 CHARACTER DISPLAY

Page 3-15

Subtest 05   320*200 Graphics display (Execution time: 4 seconds)

This test displays two sets of color blocks for the color display in the 320 x 200 dots graphics mode as shown below.

320*200 GRAPHICS DISPLAY

Subtest 06   640*200 Graphics display (Execution time: 8 seconds)

This test displays the color blocks for the black and white display in the 640 x 200 dot graphics mode as shown below.

640*200 GRAPHICS DISPLAY

Page 3-16

Subtest 07   Display page (Execution time: 15 seconds)

This test confirms that the pages can be changed in order (page 0 to page 7) in the 40 x 25 pixel mode.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³  DISPLAY PAGE 0                                   ³
³  0  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0  ³
³  0                                                0  ³
³  0                                                0  ³
³  0                                                0  ³
³  0                                                0  ³
³  0                                                0  ³
³  0                                                0  ³
³  0                                                0  ³
³  0                                                0  ³
³  0                                                0  ³
³  0                                                0  ³
³  0                                                0  ³
³  0                                                0  ³
³  0  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0  ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

Subtest 08   "H" pattern display (Execution time: 1 second)

This test displays H characters on the entire screen, as shown below.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
³HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

Subtest 09   Special attribute test

This test executes the following test.

1. EXT/FDD SW test
2. CRT, Speed, Caps,   Num, Scroll LED test
3. Attribute special test

Operations for the test is as follows.

1. After executing the test, the following message will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
```

```
³   [ EXT FDD select SW test ]           ³
³                                           ³
³   Change "EXT FDD" SW ! = [[[ OFF ]]]  ³
³                                           ³
³   Press [ENTER] KEY                    ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

Confirm that the above message [[[XXX]]] changes when it is specified by EXT FDD switch.

2. After pressing the Enter, the following message will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³   [ FONT change test ]                 ³
³                                           ³
³     Press [  Fn + -> ] key              ³
³                                           ³
³   Press [ENTER] KEY                    ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

Confirm that the font of the above message changes by pressing the Fn + -> keys.

3. After pressing the Enter, the following message will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³   [ Speed/CRT LCD test ]                               ³
³                                                           ³
³    (1) Press [  Fn + Pgdn I key ! ... Speed (red)      ³
³    (2) Press [  Fn + Pgup ] key ! ... Speed (green)    ³
³    (3) Press [  Num lock  ] key ! ...  Num (on/off)     ³
³    (4) Press [  Fn + End  ] key ! ... CRT (on)         ³
³    (5) Press [  Fn + Home ] key ! ... CRT (off)        ³
³                                                           ³
³   PRESS [ENTER] KEY                                    ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

Confirm the fact that when above combinations of keys are pressed simultaneously, the indicator showing the LED status appears on the right of each key group.

4. After pressing the Enter, the following message will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³   [ Attribute special test ]                             ³
³                                                              ³
³   (1) FG(non-zero), BG(zero)  ,R18(bit1,0) ... Double  ³
³   (2) FG(non-zero) NE BG(non-zero),R18(bit3,2)         ³
³                                                              ³
³   PRESS [ENTER] KEY                                      ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

Confirm that the character font changes by pressing Enter.

5. After pressing Enter, return to the subtest menu of the DISPLAY TEST.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.8 FLOPPY DISK TEST

CAUTION: Before running the floppy disk test prepare a formatted work disk and remove the diagnostics disk then insert the work disk to the FDD.

Subtest 01 Sequential read (Execution time: 63 seconds)

This test performs a cyclic redundancy check with a continuous read operation of all track on a floppy disk.
2D (Double-sided, double density): Track 0 to 39
2DD (Double-sided, double density, double track): Track 0 to 79

Subtest 02 Sequential read/write (Execution time: 130 seconds)

This test writes data to all tracks (as defined above) continuously and then reads the data out and compares it to original data.
(The data pattern is B5ADADH repeated.)

Subtest 03 Random address/data (Execution time: 12 seconds)

This test writes random data to random address on all tracks (as defined in subtest 01) and then reads the data out and compares it with the original data.

Subtest 04 Write specified address (Execution time: 1 second)

This test writes data specified by keyboard to tracks, heads, and address specified by the keyboard.

Subtest 05 Read specified address (Execution time: 1 second)

This test reads data from tracks, heads, and address specified by keyboard.

3.9 PRINTER TEST

CAUTION: A printer (IBM compatible) must be hooked up to the system in order to execute the test.

Subtest 01 Ripple pattern (Execution time: 110 seconds)

This test prints character for code 20H through 7EH line by line while shifting one character to the right at the beginning of each new line.

Ripple Pattern

Subtest 02 Function (Execution time: 15 seconds)

This test prints out various print type as shown below.

Normal Print
Double Width Print
Compressed Print
Emphasized Print
Double Strike Print
All Characters Print

PRINTER TEST

Subtest 03 Wrap around (Execution time: 1 second)

Note: A printer wraparound connector is necessary for executing this test. Wiring diagram of the printer wrap around connector described in the part 3.22.

Checks the data, control, and status lines with the printer wrap around connector.

LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.10 ASYNC TEST

For subtest 01 to subtest 05, transmission is done as follows in the communication.

Speed:	9600 BPS
Data:	8 bits + parity (EVEN) 1 stop bit 20H to 7EH

Subtest 01 Wrap around (channel 1) (Execution time: 1 second)

Note: An RS232C wrap around connector must be connected to channel 1 to execute this test. RS232C wrap around connector wiring diagram described in part 3.22.

Performs a data send/receive test with the wrap around connector for the channel 1.

Subtest 02 Wrap around (channel 2) (Execution time: 1 second)

Performs the same test as subtest 01 for the channel 2.

Subtest 03 Point to point (send) (Execution time: 1 second)

Note: This test can be executed on condition that the both send and receive sides are set in the same condition, and also connected together by RS232C direct cable (Wiring diagram described in part 3.22.). Subtest 03 must be executed together with subtest 04 and vice versa.

In this test, the data (20H to 7EH) are sent as one block from one side to the other, and then returned from the

later

one to the first side again. This test is used to check whether the returned data are same as the original ones.

Subtest 04 Point to point (receive) (Execution time: 1 second)

This test is exactly the same as subtest 03 except that the data flow is completely opposite.

Subtest 05 Card modem loopback (Execution time: 5 seconds)

Note: If there is no modem card in the system, this test can not be executed. Press the Fn + SysReq key, then confirm that the Built-in modem power is on.

This test is used to check whether the data, which is

from the modem to the RS232C inside the system, is same as the original data which had first been sent to the
modem
card.

Subtest 06 Card modem on-line test (Execution time: 10 seconds)

Note: After the system is connected to the PBX, unless the receive side is in the same status as the send side, the test cannot be executed. Press the Fn + SysReq key, then confirm that the Built-in modem power is on.

In this test, first some data are sent to the modem card from the RS232C inside the system, then the data is again sent to the other system through the PBX (Private Branch Exchange).
This test is used whether the returned data from the other system are same as the original data.

Subtest 07 Dial tester test (Execution time: 60 seconds)

Note: To execute this test, a dial tester must be connected to the system.

This test is carried out by sending the pulse dial and tone dial twice automatically.

[Pulse dial] : "1-2-3-4-5-6-7-8-9-0-1-2"

[Tone dial] : "1-2-3-4-5-6-7-8-9-*-0-#"

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.11 HARD DISK TEST

CAUTION: The contents of the hard disk will be erased when subtest 02, 03, 04, 06 and 08 is run. Before running the test, transfer the contents of the hard disk on the floppy disk. This can be done with the MS-DOS BACKUP command. After the test, enter the MS-DOS FDISK command, which will set the partition. Then enter the MS-DOS FORMAT command. (See the MS-DOS manual for details.)

Subtest 01 Sequential read (CYL.0-610,CYL.610-0) (Execution time: 7 minutes)

This test performs forward reading of contents from track 0 to track 610 and then performs reverse reading of the contents from track 610 to track 0.

Subtest 02 Address uniquence (Execution time: 10 minutes)

This test writes the address data(sector by sector) track by track, then reads the data and compares it to the original data.
Following three kinds of read operations are performed.
(Forward sequential, Reverse sequential, Randam)

Subtest 03 Random address/data (Execution time 48 seconds)

This test write random data in random units to random address (cylinder, head, sector) and then reads the data out and compares it to the original data.

Subtest 04 Cross talk & peak shift (Execution time: 30 seconds)

This test writes the eight types of worst pattern data (shown below) to cylinders then reads the data while shifting cylinder by cylinder.

Worst pattern data

10 Mbytes HDD	20 Mbytes HDD
1. B5ADAD	1. 6D6D
2. 4A5252	2. DBDB
3. EB6DB6	3. 6B5A
4. 149249	4. DEF6
5. 63B63B	5. D2CC
6. 9C49C4	6. 37B3
7. 2DB6DB	7. 34B5
8. D24924	8. 6DEE

Subtest 05 Write/Read/Compare (CE) (Execution time: 2 seconds)

This test writes B5ADAD warst pattern data to the CE cylinder and then reads the data out and compares it to the original data.

Subtest 06 Write specified address (Execution time: 1 second)

This test writes specified data to a specified cylinder and head.

Subtest 07 Read specified address (Execution time: 1 second)

This test reads data which has been written to a specified cylinder and head.

Subtest 08 ECC circuit (CE cylinder) (Execution time: 2 seconds)

This test checks the ECC (Error check and correction) circuit functions at the CE cylinder (Track 611).

3.12 REAL TIMER TEST

Subtest 01 Real time

A new data and time can be input during this test when the current data and time are displayed. Operations for the test is as follows.

1. After executing the test, the following message will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ REAL TIME TEST           901000 ³
³                                   ³
³ Current date: XX-XX-XXXX        ³
³ Current time: XX:XX:XX          ³
³                                   ³
³ Enter new date:                 ³
³                                   ³
³ PRESS [ENTER] KEY TO EXIT TEST  ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

2. If current date is not correct, input the current new date. Press the Enter, the Enter new time: message will appear.

3. If current time is not correct, input the current new time. Press the Enter, return to the subtest menu of the REAL TIME TEST.

Subtest 02 Real time carry

CAUTION: When this test is executed, the current data and time is erased.

This test checks whether the real-time clock increments the time displayed correctly (month, day, year, hour, minute, second).

3.13 NDP TEST

Note: This test cannot be run if there is no NDP mounted on the system PCB.
Confirm that the jumper strap is removed on the system PCB (PJ 20).
If there is no NDP mounted and is removed the jumper strap on the system PCB, system is hung up. Must be turn the POWER switch off.

Subtest 01 NDP test (Execution time: 1 second)

This test checks the control word, status word, bus, and addition/multiplication functions.

3.14 EXPANSION UNIT TEST

Note: If there is no expansion box connected to the system, this test cannot be executed.

Subtest 01 Box wrap around (8 bits bus) (Execution time: 3 seconds)

Note: As this test required a special tool to be executed, it can not be carried out here.

Subtest 02 Box mono video ram (Execution time: 1 second)

Note: If there is no monochrome display card in the expansion box, this test cannot be executed.

This test writes data (FF, AA, 55, 00H) into the monochrome display memory (B0000H to B0F9FH), then reads the data out and compares it to the original data.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.15 ERROR CODE AND ERROR STATUS NAMES

The following table shows the error code and error status names.

TABLE 3-3 Error Code and Error Status Names

DEVICE NAME	ERROR CODE	ERROR STATUS NAME
SYSTEM	01	ROM Checksum Error
	FF	Compare error
FDD	01	Bad Command
	02	Address Mark Not Found
	03	Write Protected
	04	Record Not Found
	06	Media removed on dual attach card
	08	DMA Overrun Error
	09	DMA Boundary Error
	10	CRC Error
	20	FDC Error
	40	SEEK ERROR
	60	FDD not drive
	80	Time Out Error (Not Ready)
	EE	Write buffer error
RS232C	01	DSR Off Time Out
	02	CTS Off Time Out
	04	RX EMPTY Time Out
	08	TX BUFFER FULL Time Out
	10	Parity Error
	20	Framing Error
	40	Overrun Error

	80	Line Status Error
	88	Modem Status Error
	33	NO CARRIER (CARD MODEM)
	34	ERROR (CARD MODEM)
	36	NO DIAL TONE (CARD MODEM)
PRINTER	01	Time Out
	08	Fault
	10	Select Line
	20	Out Of Paper
	40	Power off
	80	Busy Line

TABLE 3-3 Error Code and Error Status Names

DEVICE NAME	ERROR CODE	ERROR STATUS NAME
HDD	01	Bad command error
	02	Bad address mark
	04	Record not found
	05	HpC NOT RESET
	07	Drive not initialize
	09	DMA Boundary error
	0A	Bad sector error
	0B	Bad track error
	10	ECC error
	11	ECC recover enable
	20	HDC error
	40	Seek error
	80	Time out error
	AA	Drive not ready
	BB	Undefined
	CC	Write fault
	E0	Status error
	F0	Not sense error (HW.code = FF)
NDP	01	No NDP
	02	Control word error
	03	Status word error
	04	Bus error
	05	Addition error
	06	Multiplication error

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP

LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.16 HARD DISK FORMAT

There are two types of hard disk formatting:

1. Physical formatting
2. Logical formatting

This program is for physical formatting of the hard disk; it can execute the following items.

1. All track FORMAT
2. Good track FORMAT
3. Bad track FORMAT
4. Bad track CHECK

Note: Execution of the program cannot be performed unless the HDD switch is on.

CAUTION: The contents of the hard disk will be erased when this program is run. Before running the program, transfer the contents of the hard disk on to a floppy disk. This can be done with the MS-DOS BACKUP command. (See the MS-DOS manual for details.)

3.16.1 Program descriptions

1. All track FORMAT (Execution time: 6 minutes)
Performs physical formatting of hard disk in the manner shown below.

Sector sequences:	3
Cylinders:	0 to 611
Heads:	0 to 1 (10 Mbytes) 0 to 3 (20 Mbytes)
Sectors:	1 to 17
Sector length:	512 bytes per sector
Bad track unit:	10 tracks (10 Mbytes) 20 tracks (20 Mbytes)

2. Good track FORMAT (Execution time: 1 second)

Executes the formatting of a specified cylinder and track as a good track.

3. Bad track FORMAT (Execution time: 1 second)

Executes the formatting of a specified cylinder and track as a bad track.

4. Bad track CHECK (Execution time: 1 and 1/2 minutes)
Checks for bad tracks by performing a read operation for all tracks on the hard disk; a list of bad tracks is then displayed.

3.16.2 Operations

CAUTION: After physical formatting is finished, enter the MS-DOS FDISK command, which will set the partition. Then enter the MS-DOS FORMAT command. (See the MS-DOS manual for details.)

1. After pressing 2 and Enter to select from the DIAGNOSTICS MENU, the following display will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ DIAGNOSTIC - HARD DISK FORMAT                             ³
³                                                              ³
³      1 - All track FORMAT                                 ³
³      2 - Good track FORMAT                                ³
³      3 - Bad track FORMAT                                 ³
³      4 - Bad track CHECK                                  ³
³      9 - Exit to DIAGNOSTICS MENU                         ³
³                                                              ³
³ Press [NUMBER] key ?                                      ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

2. All track FORMAT Selection

(1) When All track FORMAT (1) is selected, the following message will appear.

```
Interleave number (3/1-9) ?
```

(2) Select an interleave number. (Usually select 3.) Type the number and press Enter. The following message will appear.

```
Drive number select (1:#1, 2:#2) ?
```

(3) Select a drive number. Type the drive number and press Enter. The following display will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ [HDD TYPE] : CYLINDER   = XXX                             ³
³ [HDD TYPE] : HEAD       = X                               ³
³ [HDD TYPE] : SECTOR     = XX                              ³
³                                                              ³
³ [WARNING : Current DISK data will be                      ³
³          completely destroyed]                            ³
³                                                              ³
³                              [[  cylinder,head = XXX X]]    ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

(4) After checking all cylinders of the hard disk, the following message will appear. If founds the bad track, displays the bad track number.

```
Press [Bad track number (CCCH) key ?
```

(5) If the hard disk has except the displayed the bad track number, type a bad-track number (four digits) and press Enter. (The first three digits are the cylinder number and the last digit is the head number.) If the hard disk doesn't have except them, press the Enter only. This executes the formatting of all

tracks.

(6) After formatting the hard disk, the [[cylinder, head = XXX X]] message will appear; then all cylinders of the hard disk are checked. If there is a bad track on the hard disk, the bad track number will be displayed on the screen.

(7) Format complete message will then appear.

(8) Press the Enter to return to the HARD DISK FORMAT menu.

3. Good track FORMAT or Bad track FORMAT Selection

(1) When Good track FORMAT or Bad track FORMAT is selected, the following message will appear.

```
Interleave number (3/1-9) ?
```

(2) Select an interleave number. (Usually select 3.) Type the number and press Enter. The following message will appear.

```
Drive number select (1:#1, 2:#2) ?
```

(3) Select a drive number. Type the drive number and press Enter. The following message will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ [HDD TYPE] : CYLINDER       = XXX                          ³
³ [HDD TYPE] : HEAD           = X                            ³
³ [HDD TYPE] : SECTOR         = XX                           ³
³                                                           ³
³ Press [Track Number (CCCH)] key ?                          ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

(4)Type a track number (four digits) and press Enter. (The first three digits are the cylinder number and the last digit is the head number.) This executes the formatting of good tracks or bad tracks.

Note: This program can format only one track per operation. If it is desired to format several good tracks or bad tracks, repeat the operation as many times as necessary.

(5) After formatting the track of the hard disk, the Format complete message will appear.

(6) Press the Enter to return to the HARD DISK FORMAT menu.

4. Bad track CHECK Selection

(1) When Bad track CHECK is selected, the following message will appear.

```
Drive number select (1:#1, 2:#2) ?
```

(2)Select a drive number. Type the drive number and press Enter. When the following message appears, and bad tracks of the hard disk are checked.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ [HDD TYPE] : CYLINDER       = XXX                         ³
³ [HDD TYPE] : HEAD           = X                           ³
³ [HDD TYPE] : SECTOR         = XX                          ³
³                                                           ³
³                                 [[cylinder,head = XXX X]] ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

(3)After checking the bad tracks of the hard disk are checked, the Format complete message will appear.

(4)Press the Enter to return to the HARD DISK FORMAT menu.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.17 HEAD CLEANING

3.17.1 Program description

This program executes head loading and seek/read operations for head cleaning. A cleaning kit is necessary for cleaning the FDD head.

3.17.2 Operations

1. After pressing 4 and Enter to select from the DIAGNOSTICS MENU, the following message will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ HEAD CLEANING                                             ³
³                                                           ³
³ Mount cleaning disk(s) on drive(s).                       ³
³ Press any key when ready.                                 ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

2. After the above message appears, remove the Diagnostics disk, insert the cleaning disk, and press any key.

3. When the following message appears, FDD head cleaning will begin.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ HEAD CLEANING                                             ³
³                                                           ³
³ Mount cleaning disk(s) on drive(s).                       ³
³ Press any key when ready.                                 ³
³    Cleaning start                                         ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

4. When cleaning is finished, the display automatically returns to the DIAGNOSTICS MENU.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.18 LOG UTILITIES

3.18.1 Program description

This program logs error information generated, while a test is in progress; the information is stored in the RAM.
However if the POWER switch is turned off the error information will be lost. The error information itself is displayed as the following.

1. Error count (CNT)
2. Test name (TEST)
3. Subtest number (NAME)
4. Pass count (PASS)
5. Error status (STS)
6. Address (FDD, HDD 1 or memory; ADDR)
7. Write data (WD)
8. Read data (RD)
9. Error status name

This program can store data on a floppy disk or output information to a printer.

3.18.2 Operations

1. After pressing 5 and Enter to select from the DIAGNOSTICS MENU, the error information logged in the RAM or on the floppy disk is displayed as shown below.

Error Information Display

2. Error information to be displayed on the screen can be manipulated with the following key operation.

   The 1 key scrolls the display to the next page.
   The 2 key scrolls the display to the previous page.
   The 3 key returns the display to the DIAGNOSTIC MENU.
   The 4 key erases all error log information in RAM.
   The 5 key outputs error log information to a printer.
   The 6 key reads log information from a floppy disk.
   The 7 key writes log information to a floppy disk.

3.19 RUNNING TEST

3.19.1 Program description

This program automatically runs the following tests in sequence.

1. System test (subtest number 01)
2. Memory test (subtest number 01, 02, 03, 05, 06)
3. Display test (subtest number 01 to 07)
4. FDD test (subtest number 02)
5. Printer test (subtest number 03)
6. Async test (subtest number 01, 05, 08)
7. HDD test (subtest number 01, 05, 08)

When running an FDD test, this system automatically decides whether there are one or two FDDs.

3.19.2 Operations

CAUTION: Do not forget to load a work disk. If a work disk is not loaded, an error will be generated during FDD testing.

1. Remove the diagnostics disk and insert the work disk into the floppy disk drive.

2. After pressing 6 and Enter to select from the DIAGNOSTIC MENU, the following message will appear.

```
                        Printer wrap around test (Y/N) ?
```

3. Select whether to execute the printer wraparound test (Yes) or not (No). Type the desired Y or N and press Enter key. (If Y is selected, a wraparound connector must be connected to the printer connector on the back of the unit.) The following message will appear.

```
Async wrap around test (Y/N) ?
```

4. Select whether to execute the test (Yes) or not (No). Type the desired Y or N and press Enter Key. (If Y is selected, an R5232C wraparound connector must be connected to the COMMS connector on the back of the unit.)

5. This program is repeated continuously. To stop the program, press Ctrl + Break key.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.20 FDD UTILITIES

3.20.1 Program description

These programs format and copy floppy disks, and display dump list for both the FDD and the HDD.

1. FORMAT

This program can format floppy disk (5.25"/3.5") as follows.

(a) 2D: Two-sided, double-density, 48 TPI, MFM mode, 512 bytes, 9 sectors/track.

(b) 2DD: Two-sided, double-density, double-track, 96 TPI, MFM mode, 512 bytes, 15 sectors/track.

(c) 2HD: Two-sided, high-density, double-track, 96/135 TPI, MFM mode, 512 bytes, 15 sectors/track.

2. COPY

This program copies floppy disks.

Copy with one FDD (Drive A)
Copy with two FDDs (Drive A to Drive B)

3. DUMP

This program display the contents of floppy disks (both 3.5" and 5.25") and hard disks (designated sectors).

3.20.2 Operations

1. After pressing 7 and Enter key to select from the DIAGNOSTICS MENU, the following display will appear before program execution.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ [FDD UTILITIES]                                           ³
³                                                           ³
³    1 : FORMAT                                             ³
³    2 : COPY                                               ³
³    3 : DUMP                                               ³
³    9 : EXIT TO DIAGNOSTICS MENU                           ³
³                                                           ³
³ PRESS [1] - [9] KEY                                       ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

2. FORMAT Selection

(1) When FORMAT is selected, the following message appears.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ DIAGNOSTICS - FORMAT                                      ³
³ Drive number select (1:A, 2:B) ? _                       ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

(2) Select a drive number. Type the number and the following message will then appear.

```
Type select (1:2D-04D,2:2D-08DE,3:2HD-08DE,4:2DD-2DD)
```

(3) Select a media-drive type number. Type the number and the following message will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ Warning : Disk data will be destroyed.                    ³
³                                                           ³
³ Insert work disk in to drive A:                           ³
³ Press any key when ready.                                 ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

(4) Remove the diagnostics disk from the FDD and insert the work disk; press any key.

The Format start message will appear; formatting is then executed. After the floppy disk is formatted, the following message will appear.

```
Format complete
Another format (1:Yes/2:No) ?
```

(5) If you type 1 and press Enter key, the display will return to the message in (3) above. If you type 2 the display will return

to the DIAGNOSTICS MENU.

3. COPY Selection

(1) When COPY is selected, the following message will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ DIAGNOSTICS - COPY                                        ³
³ Type select (1:2D-04D,2:2D-08DE,3:2HD-08DE,4:2DD-2DD) ? _ ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

(2) Select a media/drive type number. Type the number. The following message will then appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ Insert source disk into drive A:                          ³
³ Press any key when ready.                                 ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

(3) Remove the diagnostics disk from the FDD and insert the source disk; press any key. The Copy started message will then appear. After that, the following message will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ Insert target disk into drive A:                          ³
³ Press any key when ready.                                 ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

(4) Remove the source disk from the FDD and insert the work disk (formatted); press any key. When coping can not be done with one operation, message (2) is displayed again. Repeat the operation. After the floppy disk has been copied, the following message will appear.

```
Copy complete
Another copy (1:Yes/2:No) ?
```

(5) If you type 1 the display will return to the message in (1) above. If you type 2 the display will return to the DIAGNOSTICS MENU.

4. DUMP Selection

(1) When DUMP is selected, the following message will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ [HDD&FLOPPY DISK DATA DUMP]                               ³
³ format type select (0:2DD,1:2D,2:2HD,3:HDD) ? _           ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

2) Select a format type number. Type the number. If 3 is selected, the dump lists for the hard disk are displayed automatically.

0: Display a dump list for a floppy disk (2DD)
1: Display a dump list for a floppy disk (2D).

2: Display a dump list for a floppy disk (2HD).
3: Displays a dump list for a hard disk.

(3) If 0, 1, or 2 is selected, the following message will appear.

```
Select FDD number (1:A/2:B) ?
```

(4) Select an FDD drive number; the following message will then appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³ Insert source disk into drive A                           ³
³ Press any key when ready.                                 ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

(5) Remove the diagnostics disk from the FDD and insert a source disk; press any key. The Track number ?? message will then appear. Type the track number and press Enter.

(6) The Head number ? message will then appear. Type the head number and press Enter.

(7) The Sector number ?? message will then appear. Type the sector number and press Enter. The dump list for the floppy disk will be displayed.

(8) After a dump list appears on the screen, the Press number key (1:up,2:down,3:end) ? message will appear.

1. Displays the next sector dump.
2. Displays a previous sector dump.
3. Displays the following message.

```
Another dump (1:Yes/2:No) ?
```

(9) If you type 1 the display will return to the message shown after (4) above. If you type 2 the display will return to the DIAGNOSTICS MENU.

3.21 SYSTEM CONFIGURATION

3.21.1 Program description

This program displays the following system configuration.

1. Memory size
2. Display type
3. Floppy disk drive number
4. Async port number
5. Hard disk drive number
6. Printer port number
7. Co-processor number
8. Expanded memory port number

3.21.2 Operations

After pressing 8 and Enter key to select from the DIAGNOSTICS MENU, the following display will appear.

```
ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³       SYSTEM CONFIGURATION :                     ³
³                                                  ³
³      * - 640KB MEMORY                            ³
³      * - LCD DISPLAY                             ³
³      * - 1 FLOPPY DISK DRIVE(S)                  ³
³      * - 1 ASYNC ADAPTOR                         ³
³      * - 1 HARD DISK DRIVE(S)                    ³
³      * - 1 PRINTER ADAPTOR                       ³
³      * - 0 MATH CO-PROCESSOR                     ³
³      * - 1EXPANDED MEMORY                        ³
³                                                  ³
³       PRESS [ENTER] KEY                          ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

Press Enter key to return to the DIAGNOSTICS MENU.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

3.22 WIRING DIAGRAM

1. Printer wrap around connector

```
(9) +DATA7(4)+DATA2      ÄÄÄÄ    + SELECT       (13)

(8) +DATA6(3)+DATA1      ÄÄÄÄ    + P.END        (12)
```

```
(7) +DATA5(2)+DATA0      ÄÄÄÄ    + BUSY         (11)

(6) +DATA4(16)-INT PRT   ÄÄÄÄ    - ACKNOWLEDGE  (10)

(5) +DATA3(1)-STROBE     ÄÄÄÄ    - ERROR        (15)
```

FIGURE 3-1 Printer Wrap Around Connector

2. RS232C Wrap around connector

```
(3) TRANSMIT DATA        ÄÄÄÄÄÄÄÄ    RECEIVE DATA     (2)

(7) REQUEST TO SEND      ÄÄÄÂÄÄÄÄ    CLEAR TO SEND    (8)
                            3
                            ÀÄÄÄÄÄÄ  CARRIER DETECT   (1)

(4) DATA TERMINAL        ÄÄÄÂÄÄÄÄ    DATA SET READY   (6)
    READY                   3
                            ÀÄÄÄÄÄÄ  RING INDICATE    (9)
```

FIGURE 3-2 RS232C Wrap Around Connector

Page 3-44

3. RS232C direct cable (9-pin to 9-pin)

```
(3) TD    ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ>    RD   (2)

(4) DTR   ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÂÄÄÄÄÄÄÄÄÄÄÄÄÄÄ>    DSR  (6)
                              3
                              ÃÄÄÄÄÄÄÄÄÄÄÄÄÄÄ>    CTS  (8)
                              3
                              ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄ>    RI   (9)

(7) RTS   ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ>    CD   (1)

(5) GND   ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ    GND  (5)

(2) RD    FIGURE 3-3 RS232C Direct Cable (9-pin to 9-pin)
```

4. RS232C direct cable (9-pin to 25-pin)

```
(1) CD    ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ>    RTS  (4)

(2) RD        RD   (3)

(4) DTR   ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÂÄÄÄÄÄÄÄÄÄÄÄÄÄÄ>    CTS  (5)
                              3
                              ÃÄÄÄÄÄÄÄÄÄÄÄÄÄÄ>    DSR  (6)
                              3
                              ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄ>    RI   (22)

(5) GND   ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ   GND   (7)

(7) RTS   ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ>    CD   (8)

(6) DSR   <ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÂÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ     DTR  (20)
                         3
(8) CTS   <ÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
                         3
```

```
        (9) RI    <ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

<fig id=MMS\1200\12003_44.TIF>FIGURE 3-4 RS232C Direct Cable (9-pin to 25-pin)

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.1 GENERAL

This section gives a detailed description of the procedures used to replace FRUs (field replaceable units).

FRUs consist of the following:

1. Top Cover Assembly
2. Keyboard Unit
3. Memory Card
4. RTC Battery
5. Speaker
6. Keyboard Bridge
7. Indicator PCB
8. Built-in Modem
9. Power Supply PCB
10. FDD (Floppy Disk Drive) Base
11. FDD
12. Hard Disk Control PCB
13. Hard Disk Drive
14. System PCB
15. LCD Mask
16. LCD Module
17. LCD Cover

The following points must be kept in mind:

1. The system should never be disassembled unless there is a problem (abnormal operation, etc.).
2. Only approved tools may be used.
3. After deciding the purpose of replacing the unit, and the procedures required, do not carry out any other procedures which are not absolutely necessary.
4. Be sure to turn the POWER switch off before beginning.
5. Be sure to disconnect the ac adapter and all external cables from the system.
6. Follow only the fixed, standard procedures.

7. After replacing a unit, confirm that the system is operating normally.
8. Even if the POWER switch is turned off, the system is still supplied with electric current by the sub battery. During maintenance activity, you should take enough care so that no short circuit will occur on the system PCB.

Tools needed for unit replacement:

1. Phillips Screwdriver
2. Tweezers

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.2 REMOVING THE TOP COVER ASSEMBLY

The top cover assembly consists of the top cover (A), LCD mask (B), LCD module (C), and LCD cover (D).

Note: Replacement procedures for these items are detailed in parts 4.14 to 4.17.

FIGURE 4-1 Top Cover Assembly

1. Confirm that the POWER switch is off.

2. Turn the unit upside down and remove the seven screws (E) from the base subassembly (F).

FIGURE 4-2 Removing the Screws from the Base Subassembly

3. Turn the unit back over and remove the main battery (G) by pushing the latch release (H) to the left and lifting the battery up and out.

FIGURE 4-3 Removing the Main Battery

4. Remove the two screws (I) located beneath the main battery.

FIGURE 4-4 Removing the Screws from the Top Cover Assembly

5. Open the LCD by sliding the two side latches (J) forward while pulling the LCD upward.

FIGURE 4-5 Opening the LCD

6. The top cover assembly can now be lifted and separated from the base subassembly. Once the top cover assembly is separated from the base subassembly it should be stood on its side to the left of the unit.

FIGURE 4-6 Removing the Top Cover Assembly
from the Base Subassembly

7. To reassemble the unit, remount the top cover assembly on the base subassembly and follow the above procedures in reverse.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.3 DISCONNECTING THE TOP COVER ASSEMBLY

1. Confirm that the POWER switch is off.

2. Remove the top cover assembly as directed in part 4.2.

3. Lift the keyboard unit (A) out and place it in front of the unit.

4. Disconnect the LCD cable (B) from the system PCB (C).

FIGURE 4-7 Disconnecting the Top Cover Assembly

5. To install a new top cover assembly, follow the above procedures in reverse.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP

LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.4 REMOVING/REPLACING THE KEYBOARD UNIT

1. Confirm that the POWER switch is off.

2. Remove the top cover assembly and lift the keyboard unit out as directed in part 4.2. It is not necessary to remove the keyboard bridge (A).

3. Release the pressure plate (B) of connector PJ1 (C) to disconnect the keyboard cable from the system PCB.

FIGURE 4-8 Disconnecting the Keyboard Unit

4. To install a new keyboard unit, follow the above procedures in reverse.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.5 REMOVING/REPLACING THE MEMORY CARD, RTC BATTERY, AND SPEAKER

CAUTION: The expanded memory contents will remain in the old expanded memory. If desired, transfer the contents of the old expanded memory onto a floppy disk before replacing the memory card.
Before replacing the memory card, disconnect the sub battery from the power supply PCB.

1. Confirm that the POWER switch is off.

2. Remove the keyboard unit as directed in part 4.4.

3. Remove the single screw (A) from the memory card.

4. To disconnect the memory card cables (B), press down on the area where the cable is attached to the card and release the pressure

plates (C); then lift the card out.

5. Disconnect the two cables (D) (E) from the system PCB (F).

6. Remove the RTC battery (G) by spreading the plastic latches (H).

7. Remove the speaker (I) by pushing the plastic latch (J) outward until the speaker can be pulled out.

FIGURE 4-9 Removing the Memory Card, RTC Battery, and Speaker

8. To install a new memory card, RTC battery, and speaker, follow the above procedures in reverse.

MODEL:T1200F/FB

LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.6 REMOVING/REPLACING THE KEYBOARD BRIDGE AND INDICATOR PCB (PRINTED CIRCUIT BOARD)

1. Confirm that the POWER switch is off.

2. Remove and disconnect the top cover assembly and lift out the keyboard unit as directed in parts 4.2 and 4.3. It is not necessary to disconnect the keyboard cable.

3. Disconnect the two cables (A) and (B) from the system PCB (C).

4. Lift up the keyboard bridge (D) and disconnect the LED cable (E) from the system PCB.

5. To remove the indicator PCB (F) from the keyboard bridge, remove the single screw (G) and push the plastic latch (H) outward; pull the top edge (I) of the indicator PCB upward and outward.

FIGURE 4-10 Removing the Keyboard Bridge and Indicator PCB

6. To install a new keyboard bridge and indicator PCB, follow the above procedures in reverse.

NOTE: The LCD cable (E) and the two cables from the power supply PCB (A and B) MUST PASS THROUGH the keyboard bridge when connected.

4.7 REMOVING/REPLACING THE BUILT-IN MODEM

1. Confirm that the POWER switch is off.

2. Remove and disconnect the top cover assembly and lift out the keyboard unit and keyboard bridge as directed in parts 4.2, 4.3, and 4.6. (It is not necessary to disconnect the keyboard cable and indicator cable.)

3. Remove the line jack (A) from its mounting on the back of the FDD base (B).

4. To remove the built-in modem (C) from the system PCB (D), remove the single screw (E).
   At this time, remove the metal FG (frame ground) from the base subassembly.

FIGURE 4-11 Removing the Built-In Modem

5. To install a new built-in modem (PCB FLOMD1), follow the above procedures in reverse.

4.8 REMOVING/REPLACING THE POWER SUPPLY PCB

1. Confirm that the POWER switch is off.

2. Remove the top cover assembly as directed in part 4.2.

3. Disconnect the two forward cables (A) from the system PCB. DO NOT disconnect them from the power supply PCB (B).

4. Disconnect the remaining three cables (C) from the power supply PCB.

FIGURE 4-12 Disconnecting the Power Supply PCB Cables

5. Remove the three screws (D) and slide the power supply PCB forward to remove it.

FIGURE 4-13 Removing the Power Supply PCB

6. To install a new power supply PCB (FLOPS1), follow the above procedures in reverse.

NOTE: The two forward cables (A) MUST PASS THROUGH the keyboard bridge when connected.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.9 REMOVING/REPLACING THE FDD (FLOPPY DISK DRIVE) BASE

1. Confirm that the POWER switch is off.

2. Remove the power supply PCB as directed in part 4.8. Also remove the power panel (A) with the two screws (B). Then, remove the keyboard unit and keyboard bridge as directed in parts 4.4 and 4.6. (It is not necessary to disconnect them.)

3. Disconnect the expansion bus connector (C) and remove the line jack (D) from its mounting on the back of the FDD base (E).

4. If replacing the FDD base, remove the sub battery (F) from the rear of the FDD base.

5. Demount the built-in modem (G) from connector PJ8 and lay it on the system PCB. (It is not necessary to disconnect it.)

FIGURE 4-14 Disconnecting the Line Jack and Removing the Sub Battery

6. Remove the three screws (H) from the FDD base.

7. After disconnecting the FDD cable (I) from the system PCB, gently lift the FDD base up and toward the front of the unit.
   At this time, remove the HDD mask panel (J) from the FDD base.

8. To remove the expansion bus cable (K), remove the two screws (L) from the FDD base.

FIGURE 4-15 Removing the FDD Base

9. To install a new FDD base, follow the above procedures in reverse.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.10 REMOVING/REPLACING THE FDD

1. Confirm that the POWER switch is off.

2. Remove the FDD base as directed in part 4.9.

3. Remove the three flatheaded countersunk screws (A) and the FDD GND (B) from the FDD base.

FIGURE 4-16 Removing the FDD

4. To install a new FDD, follow the above procedures in reverse.

NOTE: Make sure to place the FDD cable in the location provided for it on the FDD base.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG

LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.11 REMOVING/REPLACING THE HARD DISK CONTROL PCB

1. Confirm that the POWER switch is off.

2. Remove and disconnect the top cover assembly and lift out the keyboard unit and keyboard bridge as directed in parts 4.2, 4.3, and 4.6. (It is not necessary to disconnect them.)

3. Remove the single screw (A) and remove the hard disk control PCB (B) from the system PCB (C).

4. To remove the hard disk control PCB from the hard disk drive (D), disconnect the hard disk drive connector (E).

FIGURE 4-17 Removing the Hard Disk Control PCB

4. To install a new hard disk control PCB, follow the above procedures in reverse.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.12 REMOVING/REPLACING THE HARD DISK DRIVE

CAUTION: The hard disk contents will remain in the old hard disk. If desired, transfer the contents of the old hard disk onto a floppy disk before replacing the hard disk. This can be done with the MS-DOS BACKUP command. (See the MS-DOS manual for details.)

1. Confirm that the POWER switch is off.

2. Turn the unit upside down and remove the seven screws (A) and three flatheaded countersunk screws (B) from the base subassembly.

FIGURE 4-18 Removing the Screws from the Base Subassembly

3. Remove the FDD base as directed in part 4.9.

4. Disconnect the cable (C) from the hard disk control PCB (D) and lift the HDD (E) out.

FIGURE 4-19 Removing the Hard Disk Drive

5. To install a new hard disk drive, follow the above procedures in reverse.

6. Format the new hard disk with MS-DOS (FORMAT C/S).

4.13 REMOVING/REPLACING THE SYSTEM PCB

1. Confirm that the POWER switch is off.

2. Remove the FDD base and hard disk control PCB as directed in parts 4.9 and 4.11.

3. To disconnect the I/O PCB (A) from the system PCB, remove the single screw (B). At this time, also remove the mask panel (C).

4. Disconnect the speaker cable (D) and RTC battery cable (E) from the system PCB.

5. To remove the system PCB and the memory card from the base subassembly, remove the four screws (F) and lift the system PCB out.

6. Remove the memory card from the system PCB as directed in part 4.5.

FIGURE 4-20 Removing the System PCB

7. To install a new system PCB (PCB SET), follow the above procedures in reverse.

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.14 REMOVING/REPLACING THE LCD MASK

1. Confirm that the POWER switch is off.

2. Open the LCD by sliding the two side latches (A) forward while pulling upward.

FIGURE 4-21 Opening the LCD

3. Using tweezers or a fine-pointed instrument, peel off the TOSHIBA label (B) and keep it in a clean place.

4. Remove the single flatheaded countersunk screw (C) and take the LCD mask (D) off by pulling it slightly forward and upward.

FIGURE 4-22 Removing the LCD Mask

5. To install a new LCD mask, follow the above procedures in reverse.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.15 REMOVING/REPLACING THE LCD MODULE

1. Confirm that the POWER switch is off.

2. Remove the LCD mask from the LCD cover subassembly as directed in part 4.14.

3. Remove the four screws (A) on the LCD module (B).

FIGURE 4-23 Removing the LCD Screws

4. Disconnect the LCD cable (C) from the LCD module.

FIGURE 4-24 Removing and Disconnecting the LCD Module

5. To install a new LCD module, follow the above procedures in reverse.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.16 REMOVING THE LCD COVER SUBASSEMBLY

1. Confirm that the POWER switch is off.

2. Remove the LCD mask and LCD cover subassembly as directed in parts 4.14 and 4.15.

3. Using tweezers or a fine-pointed instrument, peel off the hinge label (A) and remove the two screws (B) that it conceals. Keep the label in a clean place.

FIGURE 4-25 Removing the LCD Cover Subassembly Screws

4. Move the LCD cover subassembly (C) forward again to free it from the unit's top cover (D).

FIGURE 4-26 Removing the LCD Cover Subassembly

5. Remove the hinge cover (E) and the torsion bar (F) from the top cover.

FIGURE 4-27 Removing the Hinge Cover and Torsion Bar

6. Replacement procedures are described in part 4.18.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

4.17 REPLACING THE LCD COVER SUBASSEMBLY

1. Confirm that the POWER switch is off.

2. Insert the torsion bar (A) into the hole (B) provided in the top cover. Make sure that the torsion bar is fully seated before proceeding; the hooked portion should be positioned vertically.

FIGURE 4-28 Inserting the Torsion Bar

3. Insert the short end of the hinge cover plastic cable shield (C) into the main unit; the torsion bar must be seated in the hinge cover between the cover and the shield. The hinge cover itself should be seated on the two pirot ends (D).

FIGURE 4-29 Seating the Hinge Cover

4. Insert the long end of the hinge cover cable shield into the LCD cover (E).

5. Insert the short end of the LCD cover cable shield into the main unit. The cable should be sandwiched between the two shields (F).

6. While feeding the long end of the hinge cover cable shield into the LCD cover, seat the LCD cover subassembly under the two dowel ends (G).

FIGURE 4-30 Seating the LCD Cover

7. Rotate the LCD cover assembly to a vertical position while constantly maintaining pressure to prevent separation of the hinge cover and the LCD cover. Insert and tighten down the two LCD cover screws to complete the replacement procedure.

8. As directed in part 4.16, reassemble the LCD cover.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP

LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

5.1 SYSTEM UNIT

5.1.1 Inside the system unit

(A) LCD

(B) Top cover assembly

(C) Keyboard bridge

(D) Keyboard unit

(E) Power supply PCB

(F) Sub battery

(G) 3.5-inch floppy disk drive

(H) 3.5-inch hard disk drive

(I) Built-in modem

(J) Hard disk control PCB

(K) System PCB

(L) Memory card

(M) RTC battery

(N) Speaker

(O) Base subassembly

FIGURE 5-1 Inside the System Unit

5.1.2 Rear panel

(A) RGB connector (9-pin D-shell)

(B) COMP connector (2-pin)

(C) Printer connector (25-pin D-shell)

(D) Line jack (for built-in modem)

(E) Battery pack

(F) Battery lock

(G) HDD switch

(H) DC in jack (dc 12 V)

(I) Power switch

(J) Expansion slot

(K) EXP. FDD connector (25-pin D-shell)

(L) Key pad connector (2-pin)

(M) COMMS connector (9-pin D-shell)

Figure 5-2 Rear Panel

5.1.3 Left side the system unit

(A) Reset switch

(B) A-B-DIS switch

(C) LCD contrast knob

FIGURE 5-3 Left Side the System Unit

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

5.2 SYSTEM PCB

5.2.1 System PCB connectors

FIGURE 5-4 System PCB Connectors

(A) PJ 1 Keyboard connector

(B) PJ 2 System memory connector

(C) PJ 3 System memory connector

(D) PJ 4 HDC connector

(E) PJ 5 RTC battery connector

(F) PJ 6 Speaker connector

(G) PJ 7 LED connector

(H) PJ 8 Modem connector

(I) PJ 9 Power supply (HDC) connector

(J) PJ 10 Expansion bus connector

(K) PJ 11 LCD connector

(L) PJ 12 Power supply (5V) connector

(M) PJ 13 FDD (A) connector

(N) PJ 14 FDD (B) connector

(O) PJ 15 I/O connector

(P) PJ 16 Power supply (signal) connector

(Q) PJ 17 Jumper strap (HDC)

(R) PJ 18 Jumper strap

(S) PJ 19 Jumper strap

(T) PJ 20 Jumper strap (Co-processor)

(U) PJ 21 Jumper strap (Font)

5.2.2 System PCB ICs

FIGURE 5-5 System PCB ICs

(A) CPU: Central processor (80C86A-2)

(B) NDP socket

(C) BIOS ROM

(D) Gate Array (Display controller)

(E) Gate Array (PRT/FDC)

(F) Gate Array (Bus driver)

(G) Gate Array (Bus controller)

(H) Gate Array (EXP-MEM controller)

(I) FDC: Floppy disk controller (TC8565)

(J) ACE: Asynchronous communication element (TC8570)

(K) PIC: Programmable interrupt controller (82C59A)

(L) TIMER (82C54A)

(M) DMA: Direct memory access (82C37A)

(N) KBC: Keyboard controller (80C49A)

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

5.3 CONNECTORS

5.3.1 Printer connector

FIGURE 5-6 Printer Connector

TABLE 5-1 Printer Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION
1	STROB0	O	-STROBE
2	PD01	O	+DATA BIT 0
3	PD11	O	+DATA BIT 1
4	PD21	O	+DATA BIT 2
5	PD31	O	+DATA BIT 3
6	PD41	O	+DATA BIT 4
7	PD51	O	+DATA BIT 5
8	PD61	O	+DATA BIT 6
9	PD71	O	+DATA BIT 7
10	ACK0	I	-ACKNOWLEDGE
11	BUSY1	I	+BUSY
12	PE1	I	+PAPER END
13	SELEC1	I	+SELECT
14	AUTFD0	O	-AUTO FEED
15	ERROR0	I	-ERROR (FAULT)
16	PINT0	O	-PRINTER INITIALIZE

17	SLIN0	O	-SELECT INPUT
18-25	GND		GROUND (0 V)

5.3.2 EXT FDD connector

FIGURE 5-7 EXT FDD Connector

TABLE 5-2 EXT FDD Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION
1	EXRDY0	I	-EXTERNAL DRIVE READY
2	IND0	I	-INDEX
3	TR00	I	-TRACK ZERO
4	WPR0	I	-WRITE PROTECTED
5	RDA0	I	-READ DATA
6	DSKC0	I	-DISK CHANGE
7-9			(NOT USED)
10	DSELB0	O	-DRIVE SELECT
11	MONB0	O	-MOTOR ON
12	FDCWD0	O	-WRITE DATA
13	FDWE0	O	-WRITE ENABLE
14	LOWDNS0	O	-LOW DENSITY
15	FSIDE0	O	-SIDE SELECT
16	FDIRC0	O	-DIRECTION
17	STEP0	O	-STEP
18-25	GND		GROUND (0 V)

Note

Pin Number 14 is not supported at present, but it will be supported in the near future.

5.3.3 RGB connector

FIGURE 5-8 RGB Connector

TABLE 5-3 RGB Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION
1, 2	GND		GROUND (0 V)
3	CRV1	O	+R (RED) VIDEO
4	CGV1	O	+G (GREEN) VIDEO
5	CBV1	O	+B (BLUE) VIDEO
6	CIV1	O	+I (INTENSITY) VIDEO
7	-		(NOT USED)
8	CHSY1	O	+HORIZONTAL SYNC
9	CVSY1	O	+VERTICAL SYNC

5.3.4 COMMS connector

FIGURE 5-9 COMMS Connector

TABLE 5-4 COMMS Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION
1	DCD1	I	+DATA CARRIER DETECT
2	RD0	I	-RECEIVE DATA
3	SD0	O	-SEND DATA
4	DTR1	O	+DATA TERMINAL READY
5	GND		GROUND (0 V)
6	DSR1	I	+DATA SET READY
7	RTS1	O	+REQUEST TO SEND
8	CTS1	I	+CLEAR TO SEND
9	RI1	I	+RING INDICATOR

5.3.5 COMP connector

FIGURE 5-10 COMP Connector

TABLE 5-5 COMP Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION

1	P26CP	O	COMPOSITE VIDEO
2	GND		GROUND (0 V)

5.3.6 Key pad connector

FIGURE 5-11 Key Pad Connector

TABLE 5-6 Key Pad Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION
1	GND		GROUND (0 V)
2	TENKEY 1	I/O	+TENKEY

5.3.7 Expansion bus connector (in the system unit)

TABLE 5-7 Expansion Bus Connector (A side/B side) Signal Names

PIN	SIGNAL	I/O	DESCRIPTION	PIN	SIGNAL	I/O	DESCRIPTION
1	GND		GROUND (OV)	31	A191	O	UPPER 4-BIT ADDRESS
2	VCC		+5VDC	32	SYD01	I/O	BIDIRECTIONAL 8-BIT DATA BUS
3	MVEE		-9VDC	33	SYD11	I/O	BIDIRECTIONAL 8-BIT DATA BUS
4	PVDD		+12VDC	34	SYD21	I/O	BIDIRECTIONAL 8-BIT DATABUS
5	MDSL0	O	BUILT IN MODEM SELECT	35	SYD31	I/O	BIDIRECTIONAL 8-BIT DATA BUS

```
³  6  ³  CMCK1 ³   O  ³ COMMUNICATION          ³ 36  ³ GND    ³     ³
GROUND(0V)          ³
³     ³        ³      ³ CLOCK/REFRESH          ³     ³        ³     ³
³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  7  ³  MIRQ0 ³   I  ³ MODEM INTERRUPT        ³ 37  ³ SYD41  ³ I/O ³
BIDIRECTIONAL 8-BIT ³
³     ³        ³      ³ REQUEST                ³     ³        ³     ³
DATA BUS            ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ³
³  8  ³  SPTON0³   I  ³ SPEAKER DRIVE SIGNAL   ³ 38  ³ SYD51  ³ I/O ³
BIDIRECTIONAL 8-BIT ³
³     ³        ³      ³                        ³     ³        ³     ³
DATA BUS            ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  9  ³  GND   ³      ³ GROUND(0V)             ³ 39  ³ SYD61  ³ I/O ³
BIDIRECTIONAL 8-BIT ³
³     ³        ³      ³                        ³     ³        ³     ³
DATA BUS            ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  10 ³  A0BB1 ³   O  ³ ADDRESS 0 FOR BYTE BUS ³ 40  ³ SYD71  ³ I/O ³
BIDIRECTIONAL 8-BIT ³
³     ³        ³      ³                        ³     ³        ³     ³
DATA BUS            ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ³
³  11 ³  A011  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 41  ³ MEWR0  ³   O ³
MEMORY WRITE        ³
³     ³        ³      ³                        ³     ³        ³     ³
COMMAND             ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  12 ³  A021  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 42  ³ XMERD0 ³   O ³
MEMORY READ         ³
³     ³        ³      ³                        ³     ³        ³     ³
COMMAND             ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  13 ³  A031  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 43  ³ GND    ³     ³
GROUND(0V)          ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  14 ³  A041  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 44  ³ XIOWR0 ³   O ³
I/O WRITE COMMAND   ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  15 ³  A051  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 45  ³ XIORD0 ³   O ³
I/O READ COMMAND    ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  16 ³  A061  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 46  ³ TC1    ³   O ³
TERMINAL COUNT      ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  17 ³  A071  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 47  ³ CALE1  ³   O ³
CPU ADDRESS LATCH   ³
```

```
³     ³        ³      ³                        ³     ³        ³     ³
ENABLE              ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  18 ³  GND   ³      ³ GROUND(0V)             ³ 48  ³ RESET1 ³   O ³
RESET HIGH-ACTIVE   ³
³     ³        ³      ³                        ³     ³        ³     ³
OUTPUT              ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  19 ³  A081  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 49  ³ DACK10 ³   O ³
DMA ACKNOWLEDGE     ³
³     ³        ³      ³                        ³     ³        ³     ³
SIGNAL              ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  20 ³  A091  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 50  ³ IRQ21  ³   I ³
INTERRUPT REQUEST   ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  21 ³  A101  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 51  ³ GND    ³     ³
GROUND(0V)          ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  22 ³  A111  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 52  ³ VCC    ³     ³
+5VDC               ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  23 ³  A121  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 53  ³ CPCKB1 ³   O ³
CPU CLOCK           ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  24 ³  A131  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 54  ³ IRQ51  ³   I ³
INTERRUPT REQUEST   ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  25 ³  A141  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 55  ³ DRQ31  ³   I ³
DMA REQUEST         ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  26 ³  A151  ³   O  ³ LOWER 16-BIT ADDRESS   ³ 56  ³ DACK30 ³   O ³
DMA ACKNOWLEDGE     ³
³     ³        ³      ³                        ³     ³        ³     ³
SIGNAL              ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  27 ³  GND   ³      ³ GROUND(0V)             ³ 57  ³ CPADE0 ³   O ³
CPU ADDRESS ENABLE  ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  28 ³  A161  ³   O  ³ UPPER 4-BIT ADDRESS    ³ 58  ³ DRQ11  ³   I ³
DMA REQUEST         ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  29 ³  A171  ³   O  ³ UPPER 4-BIT ADDRESS    ³ 59  ³ IORDY1 ³   I ³
I/O CHANNEL READY   ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  30 ³  A181  ³   O  ³ UPPER 4-BIT ADDRESS    ³ 60  ³ GND    ³     ³
GROUND (0V)         ³
```

TABLE 5-8 Expansion Bus Connector (C side/D side) Signal Names

PIN	SIGNAL	I/O	DESCRIPTION	PIN	SIGNAL	I/O	DESCRIPTION
1	-		NOT USED	21	-		NOT USED
2	-		NOT USED	22	GND		GROUND(0V)
3	-		NOT USED	23	DACK00	O	DMA ACKNOWLEDGE SIGNAL
4	-		NOT USED	24	-		NOT USED
5	-		NOT USED	25	-		NOT USED
6	-		NOT USED	26	-		NOT USED
7	-		NOT USED	27	-		NOT USED
8	-		NOT USED	28	IOERR0	I	I/O ERROR
9	-		NOT USED	29	-		NOT USED
10	GND		GROUND(0V)	30	GND		GROUND(0V)
11	-		NOT USED	31	-		NOT USED

```
³  12 ³  -     ³      ³ NOT USED          ³ 32  ³ DACK20 ³     ³ DMA
ACKNOWLEDGE     ³
³     ³        ³      ³                   ³     ³        ³     ³ SIGNAL
³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  13 ³  IRQ61 ³   I  ³ INTERRUPT REQUEST ³ 33  ³ -      ³     ³ NOT
USED            ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  14 ³  -     ³      ³ NOT USED          ³ 34  ³ -      ³     ³ NOT
USED            ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  15 ³  -     ³      ³ NOT USED          ³ 35  ³ -      ³     ³ NOT
USED            ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  16 ³  -     ³      ³ NOT USED          ³ 36  ³ -      ³     ³ NOT
USED            ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  17 ³  DRQ21 ³   O  ³ DMA REQUEST       ³ 37  ³ MDSL0  ³   O ³ BUILT
IN MODEM      ³
³     ³        ³      ³                   ³     ³        ³     ³
SELRCT           ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  18 ³  -     ³      ³  NOT USED         ³ 38  ³ -      ³     ³ NOT
USED            ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  19 ³  -     ³      ³ NOT USED          ³ 39  ³ IRQ71  ³   I ³
INTERRUPT REQUEST   ³
ÃÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÅÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³  20 ³  -     ³      ³ NOT USED          ³ 40  ³ GND    ³     ³ GROUND
(0V)          ³
ÀÄÄÄÄÄÁÄÄÄÄÄÄÄÄÁÄÄÄÄÄÄÁÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÁÄÄÄÄÄÁÄÄÄÄÄÄÄÄÁÄÄÄÄÄÁÄÄÄÄÄÄÄÄ
ÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

5.4 KEYBOARD LAYOUT

5.4.1 USA version

FIGURE 5-12 USA Version

5.4.2 England version

FIGURE 5-13 England Version

5.4.3 German version

FIGURE 5-14 German Version

5.4.4 France version

FIGURE 5-15 France Version

5.4.5 Spain version

FIGURE 5-16 Spain Version

5.4.6 Italy version

FIGURE 5-17 Italy Version

5.4.7 Scandinavia version

FIGURE 5-18 Scandinavia Version

5.4.8 Switzerland version

FIGURE 5-19 Switzerland Version

5.4.9 Keycap number

FIGURE 5-20 Keycap Number

MODEL:T1200F/FB

LANG:TAIS

LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

5.5 DISPLAY CODE

TABLE 5-9 Display Code

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

A.1 GENERAL

The Bus Controller Gate Array is a 2,000 gate flat package type chip with 100 lead pins. It contains the following functions. Signal name and meaning of each pin used in this chip are explained in this section together with its detailed definitions.

1) Clock generator
2) Command decoder
3) Bus controller
4) 8-16 bit controller
5) Wait controller
6) DMA bus controller
7) DMA page register
8) RAM/ROM select controller
9) NMI controller
10) Keyboard controller
11) Circuitry compatible with the 8255

FIGURE A-1 Bus Controller G.A.

A.2 BLOCK DIAGRAM

FIGURE A-2 Block Diagram

MODEL:T1200F/FB

A.3 PIN DESCRIPTION

TABLE A-1 Pin Description

Pin	I/O	SYMBOL	Signal name and Description
1	I/O	D7	IOD71 Bidirectional data bus bit 7
2	I/O	D6	IOD61 Bidirectional data bus bit 6
3		Vcc	+ 5V
4	I	A01	A011 Address bit line 0
5	I	A0B	A0B1 Address bit 0 for byte bus
6	I	A13	A131 Address bit 13
7	I	A14	A141 Address bit 14

8	I	A15	A151 Address line bit 15
9	I/O	A16	A161 Address line bit 16
10	I/O	A17	A171 Address line bit 17
11	I/O	A18	A181 Address line bit 18
12	I/O	A19	A191 CPU/DMA address lines. CPU address is input when input mode. DMA page register content is output when output mode (DMA cycle). Address line bit 19
13	O	BDLEN	BDLEN0 Byte bus low enable (enable signal for byte read/write operation.

Pin	I/O	SYMBOL	Signal name and Description
14	I	DACKO	DACK00 DMA acknowledge signal for channel 0
15		GND	Ground
16	I/O	IOR	IORD0 I/O bus data read command
17	I/O	IOW	IOWR0 I/O bus data write command
18	O	RESET	RESET0 Reset active low output
19	I	BHE	BHE0 Bus high enable
20	I		S20 CPU status signal bit 2
21	I		S10 CPU status signal bit 1
22	I		S00 CPU status signal bit 0
23	I/O	CRG0	CRG00 This gate sends a low pulse to RQ/GT pin of the CPU when the GA receives a HRQDM1 signal from the 82C37. Then it

			sends a HOLDA1 signal to the 82C37 when it receives a low pulse to the CPU from this gate when the DMA cycle is completed.
24	O	ROMCS	ROMCS0 ROM select signal (ROM = F0000 - FFFFF)
25	I/O	BAMCS	BAMCS0 Back up memory chip select
26	I/O	A0BB	A0BB1 Address 0 for byte bus (Buffer)
27	I/O	XIOR	XIORD0 I/O read command (Buffer)

Pin	I/O	SYMBOL	Signal name and Description
28		Vcc	+ 5V
29	I	XIOW	XWOIR0 I/O write command (Buffer)
30	O	XMEMW	XMEWR0 Memory write command
31	O	CPADE	CPADE0 CPU address enable
32	O	PRDY	PRDY1 CPU ready signal
33	I	RESET	RESET1 Reset pulse. This signal is active high.

34	I	KBCL	KBCL1 Clock signal from the key board controller. This is used to transfer data from the keyboard controller.
35	I	KBDT	KBDT1 Data from the keyboard controller.
36	I	87ON	87ON1 8087 installed
37	I	INT87	INT871 8087 interactive
38	I	KSCLK	KSCLK1 Keyboard status clock
39	I	KSDAT	KSDAT1 Keyboard status data
40		GND	Ground
41	O	KBCLK	KBCLK1 Data transfer clock to the keyboard controller. Low level at Port-B bit6 = "0"

Pin	I/O	SYMBOL	Signal name and Description
42	O	KBDTA	KBDTA1 Data to the keyboard controller
43	O	NMI	NMI1 Non maskable iterrupt
44	O	NUML	NUML1 NUM lock status
45	O	FAST	FAST1 CPU clock mode ("High" 9.54 MHz, "low" = 4.77 MHz)
46	I	TEST 1	PO3A0 Output command inhibit signal
47	I	TEST 2	PO3B0 Test mode selection 2
48	I	TEST 3	PO3C0 Test mode selection 3
50	O	DRQ0	DRQ01 DMA request for CH0
51	O	IRQ1	IRQ11 Interrupt Request level 1 signal. (for the keyboard interrupt)

52	O	TMGAT	TMGAT1 Control signal to the gate 2 of the 82C53.
53		Vcc	+ 5V
54	O	TMCLK	TMCLK1 Clock signal for the 82C53
55	O	CPCKB	CPCKB1 CPU clock buffer

Pin	I/O	SYMBOL	Signal name and Description
56	I	IOER	IOERR0 I/O error. It is low active.
57		TC2	TC2OUT1 Output signal from the channel 2 of the 82C53.
58	O	DRDY	DRDY1 Bus ready signal during the DMA cycle.
59	I/O	INTA	INTA0 Interrupt acknowledge signal
60	I	RERQ	RERQ1 Refresh request
61	I/O	DMER	MERD0 Memory data read command
62	I	DHRQ	DHRQ1 DMA hold request signal from the 82C37
63	I	DACK3	DACK30 DMA acknowledge signal for channel 3
64	O	SPKDR	SPKDR0 Speaker Drive signal
65		GND	Ground

66	O	RASTL	RASTL0 RAS Strobe Timing Low signal
67	O	RASTH	RASTH0 RAS Strobe Timing High signal
68	I	DACK2	DACK20 DMA acknowlegde signal for channel 2
69	I	PSNMI	PSNMI1 Power supply NMI
70	I	EXMSL	EXMSL0 Expanded Memory Select signal
71	O	DMCLK	DMCLK1 DMA clock

Pin	I/O	SYMBOL	Signal name and Description
72	I	AEN	DMAEN DMA address enable signal. This signal is generated from the AEN signal of the 82C37
73	O	CPCLK	CPCLK1 CPU Clock : 4.77 MHz (Slow) 9.54 MHz (Fast)
74	O	XMEMR	XMERD0 Memory read command
75	I/O	MEMW	MEWR0 Memory write command
76	I	RDY	IORDY1 I/O ready signal
77	O	DMSL	DMSEL0 V-RAM select signal
78		Vcc	+ 5V
79	O	ECRT	FLTDSL1 Flat display select signal
80	O	DFNT	CHFONT0 Double font select signal
81	O	IODMS	IODMS0 IOD Bus memory select signal
82	I	MCRCS	MCRCS0 Machine control register chip select
84	O	BWDIR	BWDIR1

			Specifies data direction. Held to be low except IOWR and MEMW to the I/O bus.
85	1	A00	A001 Address line bit 0

Pin	I/O	SYMBOL	Signal name and Description
86	I	NMIRG	NMICS0 NMI mask register chip select
87	I	PAGWR	PAGWR0 DMA page register write signal
88	O	WDLAT	WDLAT1 Low data (even) latch signal for word read operation to 8-bit bus.
89	O	WDLEN	WDLEN0 Low data (even) enable signal for word read operation to 8-bit bus.
90		GND	Ground
91	I	OSC	SC141 Output from the OSC. 14.31818MHz.
92	I	PPICS	PPICS0 PPI select signal. This signal is active low.
93	O	CALE	CALE1 CPU address latch enable signal
94		HLDA	HLDA1 Hold acknowledge
95	I/O	D0	IOD01 Bidirectional data bus bit 0
96	I/O	D1	IOD11 Bidirectional data bus bit 1
97	I/O	D2	IOD21 Bidirectional data bus bit 2
98	I/O	D3	IOD31 Bidirectional data bus bit 3
99	I/O	D4	IOD41 Bidirectional data bus bit 4
100	I/O	D5	IOD51 Bidirectional data bus bit 5

A.4 DESCRIPTIONS OF EACH FUNCTION

Following are the summarized description about each functional block in this gate array.

A.4.1 Clock generator

The clock generator receives 14.31818MHZ clock, then generates the CPU clock, DMA clock and Timer clock.

CPU clock : 4.77MHz/9.54MHz*
DMA clock : 4.77MHz (Duty 50%)
Timer clock : 1.18MHz (Duty 50%)

* CPU clock rate is changed by selecting one of the two modes (Fast/Low).

A.4.2 Command decoder

Commands to the I/O controller or memory are generated by decoding the CPU status.

TABLE A-2 Command Decoder

S2	S1	S0	Command
0	0	0	INTA0
0	0	1	IORD0
0	1	0	IOWR0
0	1	1	(None)
1	0	0	MERD0
1	0	1	MERD0

1	1	0	MEWR0
1	1	1	(None)

A.4.3 Bus controller

The bus controller controls the data bus by decoding commands mentioned above.

A.4.4 8-16 bit conversion controller

8 bit-16 bit conversion is performed by this circuitry when an 8-bit bus is accessed. The bus wait timing is controlled by this circuitry.

A.4.5 Wait controller

The wait controller decodes the CPU wait cycle according to each command described on the previous page by the Bus Ready signal.

A.4.6 DMA bus controller

The DMA bus controller issues the DMA request signal and controls the bus. It issues a bus disconnection request signal (RQ/GT) to the CPU as a response to the DMAS request from the DMAC.

It issues HOLDA1 signal to the DMAC when the bus is disconnected, then the DMA cycle starts. After the DMA cycle is completed, it changes the bus connection to the CPU by sending a signal to the RQ/GT gate of the CPU.

A.4.7 DMA Page register

This register is to save the upper 4 bits of the address lines (A19-A16) during the DMA cycle.
This is composed of 3 sets of 4-bit registers and they are assigned to the following I/O addresses.

TABLE A-3 DMA Page Register

I/O Address	Command	Description
081	IOWR	DMA channel 2 page register 7 ── ── ── ── 4 3 2 1 0 A19 A18 A17 A16
082	IOWR	DMA channel 3 page register
083	IOWR	DMA channel 1 page register

A.4.8 RAM/ROM select controller

This circuitry is for RAM/ROM select control on the system board and issues RAS/CAS signals to the RAM and ROM for the control.

RAM and ROM selection is performed by decoding the address line data.

A.4.9 Keyboard data controller

This circuitry is to receive bit-serial data from the keyboard controller (80C49), then the data is converted to parallel data. If the PB7 is "0", the converted parallel data is output to the PA, but if the PB7 is "1", the output is disabled and the keyboard data is cleared. When the PB6 is "0", the keyboard data is inhibited but if it is "1", it gets enabled. The keyboard data is composed of 8 bit-data with a leading start bit total of 9 bits. When the circuitry receives one-byte data from keyboard controller, it inhibits from receiving more data and issues interrupt signal (IRQI).

A.4.10 Circuitry compatible with 8255

This circuitry is compatible with the intel 8255 (PPI) chip. It contains Port-A, B, A and some control registers.

a) Port A (I/O address = 060H)
Data setting to the register is performed by writing to the I/O address 060H.
Getting the data from the register is performed by reading the same address after setting 0 to bit 4 of the mode register. Bit 4 of the mode register is usually set to "1" (when power on reset) and the following data is acquired when read operation is executed.

When mode register bit4 = "1"

A.4.11 DMA page register

This register is to save the upper 4 bits of the address lines (A19-A16) during the DMA cycle.
This is composed of 3 sets of 4-bit registers and they are assigned to the following I/O addresses.

b) Port B (I/O address = 061H)
Data setting to the register is performed by writing to the I/O address 061H.
Getting the data from the register is performed by reading the same address. The meaning of each bit of the register is as follows.

When mode register bit4 = "1"

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³        ³  Bit  ³           Description                 ³
ÃÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³        ³PA 0   ³   + Timer 2 Gate speaker              ³
³    I   ³       ÃÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
```

	1	+ Speaker data
N	2	Not used
P	3	Read high/Low switch
	4	- Enable RAM parity check
U	5	- Enable I/O channel check
T	6	- Hold keyboard CLK low
	7	- (Enabled keyboard)

Each bit of the register (PC bit) after power on reset is as follows;

BIT	7	6	5	4	3	2	1	0
State	1	0	1	1	1	1	0	0

c) Port C (I/O address = 062H)
Data setting to the register is performed by writing to the I/O address 062H.
Acquiring the data from the register is performed by reading the same address when bit 0 (PC0-3) and bit 3 (PC4-7) of the mode control register are set to "0".
Bit 0 and 3 of the mode register are usually set to "1" (when power on reset) and the following data is acquired when read operation is executed.

When mode register bit 4 = "1"

	Bit	PB7 = "0"	PB7 = "0"
I	PA 0		
N	1		
P	2	Keyboard	
U	3	input	
T	4	data	
	5		
	6		
	7		

d) Mode control register (I/O address = 063H)
This register is set as follows by writing the data to the address 063H, or by resetting the power on.

BIT	7	6	5	4	3	2	1	0
State	1	-	-	1	1	-	-	1

Bit	Bit	Description
0	0	PC latch data (PC0-3) is selected as read data of PC0-3.
	1	SW data is selected as read data of PC0-3.
3	0	PC latch data (PC4-7) is selected as read data of PC4-7.
	1	Status information is selected as read data of PC4-7.
4	0	PA latch data is selected as read data of PA.
	1	KB data is selected as read data of PA.
7	0	Not used
	1	Enable to set mode control register. Resets PortA, PortB, PortC.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP

B.1 GENERAL

I/O driver gate array is composed of two main controllers; FDD controller, and PRT controller, each of which is explained individually in this section.

This G.A. (Gate Array) contains 100 pins altogether and the functions or devices of each controller are as follows;

a) FDD Controller

- Digital Input Register (3F7H Read)
- Digital Output Register (3F2H Write)
- X-Rate Register (3F7H Write)
- DMA Request Delay
- Write Precompensation
- FDC Chip Select

b) Printer Controller

- Data Register (378H Read/Write)
- Status Register (379H)
- Control Register (37AH)

The detailed explanation about each pin is also given together with its block diagram.

B.2 BLOCK DIAGRAM

FIGURE B-1 PRT/FDD Gate Array Block Diagram

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

B.3 PIN DESCRIPTION

TABLE B-1 Pin Description

Pin	I/O	SYMBOL	Signal name and Description
01	O	AUTF	AUTFD1: When this bit is set to "1", the set paper is automatically fed one line after the printing is finished.
02	O	STRB	STROB1: Strobe signal used when data is sent to the printer
03		Vcc	+ 5 v dc
04		GND	Ground
05	I	TEST2	P12A0: Testpin. (Not used)
06	I	TEST1	P12B0: Testpin. (Not used)
07	I	HRESET	HRESETO HDD reset
08	I	XINT	XINT1: Interrupt Request from the HDC
09	I	HDDSL	HDDSL0: HDD select signal
10	O	HRST	HRST1: HDD Reset signal
11	O	IRQ5	IRQ51: Interrupt Request 5 signal
12	O	HDCS	HDCSO: HDC chip select signal
13	O	HDIR	HDIR1: Direction of the system data bus towards HDC
14			N.C
15		GND	Ground
16			N.C
17	O	FDRDY	FDRDY1: When FDD is selected, this signal becomes FDRDY1, that is, "OR" for both of DSLB and DSLA
18	O	DRQ2	DRQ21: DMA request to 82C37, but is suspended

19	O	IRQ6	IRQ61: Interrupt request to 82C59
20	O	TC1	TC1: Output signal (inverted from TC0 signal) to EXP. slot
21	I	TC0	TC0: Terminal count output from 82C37
22	I	PRTSL	PRTSL0: Printer port select signal
23	I	FDDSL	FDDSL0: FDD port select signal (3F0~3F7H)
24	O	BDLED	BDLED0: B Drive LED turn on signal
25	I	D7	SYD71: System data bus bit 7.
26	I	A0	AOB1: Address bit 0
27	I	IOW	IOWR0: I/O write command signal

Pin	I/O	SYMBOL	Signal name and Description
28			Vcc + 5 Vdc
29		GND	Ground
30	I	IORD	IORD0: I/O read command signal
31	I	A1	AO11: Address bit 1
32	I	A2	AO21: Address bit 2
33	I	RESET	RESET0: System reset

```
 ³34 ³ I ³D0     ³SYDO1: System data bus bit 0
³
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 ³35 ³ I ³D1     ³SYD11:           " bit 1
³
ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
´
 ³36 ³ I ³D2     ³SYD21            " bit 2
³
ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
´
 ³37 ³ I ³D3     ³SYD31            " bit 3
³
ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
´
 ³38 ³ I ³D4     ³SYD41            " bit 4
³
ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
´
 ³39 ³ I ³D5     ³SYDS1            " bit 5
³
ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
´
 ³40 ³   ³GND    ³Ground
³
ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
´
 ³41 ³ I ³D6     ³SYD61            " bit 6
³
ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
´
 ³42 ³ I ³DACK2  ³DACK20: Channel 2 Acknowledge signal from DMA
³
ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
´
 ³43 ³ O ³IRQ7   ³IRQ71: Interrupt request 7
³
ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
´
 ³44 ³ I ³FINT   ³FDCIT1: Interrupt request from FDC
³
ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
´
 ³45 ³ I ³FDRQ   ³FDCRQ1: DMA request from FDC
³
ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
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 ³46 ³ I ³CKFD   ³$CKFD1: Clock signal from Variable Frequency 
Oscillator³

ÃÄÄÄÄÅÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
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 ³47 ³ I ³FDCWD  ³FDCWD1 Write data signal from FDC                       
³

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 ³48 ³ I ³FDCWE  ³FDCWE1 Write enable signal from FDC                     
³

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 ³49 ³ I ³PS0    ³PSO1 Write precompensation control signal from FDC      
³

ÃÄÄÄÄÅÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
´

 ³50 ³ I ³PS1    ³PS11 "                                                  
³

ÃÄÄÄÄÅÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
´

 ³51 ³ I ³IDKCH  ³IDKCH0 Disk change signal from FDD                      
³

ÃÄÄÄÄÅÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
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 ³52 ³ I ³EFDSL1 ³When this bit is set to "1", external FDD is selected 
³

ÃÄÄÄÄÅÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
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 ³53 ³   ³Vcc    ³+ 5 V dc                                                
³

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 ³54 ³   ³GND    ³Ground                                                  
³

ÀÄÄÄÄÁÄÄÄÄÁÄÄÄÄÄÄÄÄÁÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ
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 ³Pin³I/O³SYMBOL ³Signal name and Description                            ³
 ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
 ³55 ³ I ³ EFDA  ³ EFDA0: When this is "0", external FDD is assigned to³
 ³   ³   ³       ³ Drive A                                               ³
 ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
 ³56 ³ I ³ HDDLED³ HDDLED1: HDD LED turn on signal from HDC              ³
 ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
 ³57F³ O ³ DTC   ³ FDAKT1: Terminal count output to FDC, controlled by ³
 ³   ³   ³       ³ DOR bit 3                                             ³
 ÃÄÄÄÅÄÄÄÅÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
 ³58 ³ O ³ FDACK ³ FDACK0: DMA acknowledge signal output to DMA,         ³
```

			controlled by DOR bit 3
59	O	FWDAT	FWDAT1: Write data signal with write precomp. to FDD
60	O	FDCS	FDCCS0: Chip select signal to FDC
61	O	FRES	FRST1: Reset signal to FDC, controlled by DOR bit 2
62	O	MN	MIN1: VFO (Variable Frequency Oscillator)
63	O	MFMO	LOWD0: To the MFM/FM pins of the VFO,
64	O	MFMI	LOWD1: Inverted LOWD0 output signal
65		GND	Ground
66	O	IDSLA	IDSLA0: Drive A select signal
67	O	IMONA	IMONA0: Drive A motor ON signal
68	O	IDSLB	IDSLB0: Drive B select signal
69	O	IMONB	IMONB0: Drive B select signal
70	O	EDRSL	EDRSL1: External FDD select signal
71	O	EMTON	EMTON1: External FDD motor ON signal
72	O	ADRED	ADLED0: A Drive LED turn on signal

Pin	I/O	SYMBOL	Signal name and Description
73 ~ 77, 80 ~ 82	I	IPD71~31 IPD21~01	OPD70~30, 0PD20~00: Response data, from the printer connector
83	I	RSLI	RSLIN1: LIN1 response signal from the printer connector
84	I	RAUT	RATFD1: AUTFD1 response signal from the printer connector
85	I	BUSY	IBSY1: When this bit is set to "1", the printer is busy.
86	I	ACK	IACK0: When the printer is ready to receive the next data, this bit is set to "0" for 5æs. Normally it is set to "1".
87	I	PE	IPE1: When this bit is set to "1", the printer is in the state of "End of paper".
88	I	SEL	ISLCT1: When this bit is set to "1", the printer is

			in the state of "selected".
89	I	ERR	IERR0: When this bit is set to "0", the printer is in the state of either "Paper end", "off line", or of "error".
90		GND	Ground
91 ~ 98	O	OPD7~0	OPD70~00: Output of data or data register to the printer
99	O	SLIN	SLIN1: When this signal is "1", printing is enabled.
100	O	PINT	PINT1: When this bit is set to "1", printer is initialized.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

B.4 FUNCTIONS OF THE FDD CONTROLLER

B.4.1 Digital input register (3F7H Read)

Bit	7	6	5	4	3	2	1	0
	DSCH	EXTB	EXTA	DSL	Not used			

- DSCH (Disk Change)

  When this bit (bit 7) is set to "1", it indicates that the used disk may have been changed. This bit is effective only when internal 3.5-inch FDD is used, and when the external FDD is used, this bit is always set to "O".

- EXTB (External FDD B)

  When this bit (bit 6) is set to "1", the external FDD Sel switch is set to Drive B.

- EXTA (External FDD A)

When this bit (bit 5) is set to "1", the external FDD Sel switch is set to Drive B.

Ext. FDD Sel SW.	EFDSL1	EFDA0	Status
1-2	0	1	Ext. FDD Off
Off	1	1	Ext. FDD Drive B
2-3	1	0	Ext. FDD Drive A

+ DSL "OR" of the drive select signals A and B is output from the G.A..
This signal is used to know whether the FDD is active or not.
This is output also to the EMC-GA.

FIGURE B-2 FDD General Block Diagram

When this bit is "1", it indicates that either drive A or B is selected.

B.4.2 Digital output register (3F2H Write)

Bit	7	6	5	4	3	2	1	0
	Not used		MONB	MONA	IDEN	FRST	DSL1	DSL0

+ MONB	When this bit is "1", motor of the drive B is on.
+ MONA	When this bit is "1", motor of the drive A is on.
+ IDEN	When this bit is "1", IRQ and DRQ are enabled.
- FRST	When this bit is "0", the FDC (TC8565F) is reset.
+ DSL1 & +DSL0	When both of these bits are "0", the drive A is selected. When DSL1 is "0" and DSL0 is "1", the drive B is selected.
+ IDEN	When this bit is "1", the following signals are enabled. TC0, DACK20, DRQ21, IRQ61

B.4.3 X-Rate register (3F7H Write)

Bit	7	6	5	4	3	2	1	0
	Not used						Rate-1	Rate-0

X-Rate-1	X-Rate-0	
0	0	360rpm, 500kb/s, MFM
0	1	360rpm, 300 kb/s, MFM
1	0	300rpm, 250 kb/s, MFM
1	1	Not used

FIGURE B-3 Printer/FDD Gate Array

- Write Precompensation

Input		Output
RS1	RS0	Write data
0	0	as it is
0	1	125æs early
1	0	125æs late

- FDCCS0 Chip Select

FDC Register

Data Register	3F5H
Main Status Register	3F4H

FDCCS1 = A9ù A8ù A7ù A6ù A5ù A4ù A3ù A3ù A1

* FDDSL0 signal is sent from EMC

FDDSLO = A9ù A8ù A7ù A6ù A5ù A4ù A3ù DMA

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

B.5 FUNCTIONS OF THE PRINTER CONTROLLER

Printer Controller is mainly composed of the following three registers.

- Data Register (Read/Write 378H)
- Status Register (Read 379H)
- Control Register (Read/Write 37AH)

B.5.1 Data register output (378H)

Bit	7	6	5	4	3	2	1	0
	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0

By this register, 8-bit write data is set. These bits are sent to the printer through the driver (LSO5).

B.5.2 Data register input (378H)

By this register, the response data from the printer connector can be read.
This function is used for wraparound test, and is used also for data input from external devices connected to the connector. In this case, the driver must be set to "0". All this operation is controlled by the control register explained afterwards.

B.5.3 Status register (379H Read)

Bit	7	6	5	4	3	2	1	0
	BSY	ACK	PE	SLCT	ERR	Not used		

- Status data from the printer -

BSY - BUSY1 signal is input inverted from the printer

ACK - ACK0 is input from the printer

PE - PE1 is input from the printer

SLCT - SELEC1 is input from the printer

ERR - ERRO0 is input from the printer

B.5.4 Control Register Output (37AH Write)

Bit	7	6	5	4	3	2	1	0
	PDIR	Not used		IRQEN	SLTIN	IPRT	AUTFD	STRB

- Controlling signals -

IRQEN - When this bit is set to "1", IRQ signal from the printer port is output to the 82C59 (PIC).

PDIR - This signal decides the data transfer direction of the 8-bit data on the connector. When this bit is set to "1", input from the connector is enabled, and when "0", output from the Data Register is enabled.

STRB - This signal is inverted to be output to the connector.

AUFD - This signal is inverted to be output to the connector. This bit returns from the connector after being sent to it.

IPRT - This signal is output to the printer as it is.

SLTIN - This signal is inverted to be output to the printer. This bit returns from the connector after being sent.

B.5.5 Printer mode register (37FH Write)

Bit	7	6	5	4	3	2	1	0
	Not used							BDIS

- Direction signal -

+ BDIS (Bidirection disable)

This signal is used to control the direction of the data to or from the printer port.
When this bit is set to "0", bit 7 of the control register is disabled, and only output from the printer port is enabled.

Control Register

FIGURE B-4 Data Transfer Direction Control

MODEL:T1200F/FB

LANG:TAIS

LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

C.1 GENERAL

Bus drive gate array includes the data bus and address driver that control the buses between the CPU and memory, or the CPU and I/O devices.
This gate array also includes the decode circuit for chip select signals, by which the devices connected to the I/O bus can be selected.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

C.2 FUNCTIONS

This gate array contains the following functions.

- Latches the CPU address and data
- Switches the CPU address/data and those of the DMA.
- Controls the data transfer between the CPU and the I/O bus or the system bus.
- Decodes the I/O address
- Controls the refresh request
- Contains the back-up register for resuming.

This gate array is composed of 100 pins altogether, and details of each pin are also included in this section.

MODEL:T1200F/FB

LANG:TAIS

C.3 BUS DRIVER BLOCK DIAGRAM

FIGURE C-1 Block Diagram

- Control Signals -

Meanings of each signal described on the previous page are as follows.

- CPUDE	The direction of ODD data bus towards the CPU BDHENùBWDIR
- CPLDE	The direction of EVEN data bus towards the CPU WDLEN+BDLENùBWDIR
- ALE	Address Latch Enable
- HLDA	Holds Acknowledge signal. During the DMA cycle, this signal is active.
- IODEN	I/O data bus enable signal. When a device on the I/O data bus is accessed, this signal becomes active. HLDAù(INTA+IODMS)ùHLDAùA9ù A8ù(OCO-OD)ù(OE5-OEF) ù(IORD+IOWR)
- IODIR	I/O data bus direction signal. When this signal is "1", writing operation is enabled, and when "0", reading is enabled. ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ INTA+ IODMSùMERD+IORDùA8ùA9
- YIODEN	I/O data input/output buffer is enabled. IODIRùIODENùBWDIRù(BDLEN+BDHEN)
- SYDEN	SYD bus input/output buffer is enabled. BWDIRù(BDLEN+BDHEN)

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

C.4 1IN DESCRIPTION

TABLE C-1 Pin Description

Pin	I/O	SYMBOL	Signal name and Description
1,2	I	AD11 ~A12	AD111~A121: Two of the lower 16 bits of the data bus from the CPU, and are bidirectional
3		Vcc	+ 5V dc
4		GND	Ground
5~ 7	I	AD13 ~15	AD131~AD151: Three of the lower 16 bits of the data bus from the CPU. They are all bidirectional.
8~ 11	I	AD16 ~19	AD161~AD191: Upper 4 bits of the address bus from the CPU
12	I	RESET	RESET0: Power on reset signal
13	I	IOW	IOWR0: I/O write command signal
14	I	IOR	IORD0: I/O read command signal
15		GND	Ground
16	O	INTCS	INTCS0: Interrupt controller chip select signal
17	I	BDLEN	BDLEN0: EVEN data enable signal When WDLEN is "0", it is inhibited.
18 ~ 21	O	A19~16	A191~161: Upper 4 bits of the address bus, and during the DMA cycle, they become in the state of high impedance
22 ~ 24	O	A15~13	A151~131: Three of the lower 16 bits of the address bus, during the DMA cycle; IOD71~01??A151~081 DMAD71~01??A071~001

25	I	AOB	AOB1: Bit "0" of the system address.

Pin	I/O	SYMBOL	Signal name and Description
26	O	A01	A011: Address bit 1
27	O	IOD6	IOD61: Bidirectional I/O data bus
28		Vcc	+ 5V dc
29		GND	Ground
30	O	IOD7	IOD71: Bidirectional I/O data bus
31		GND	Ground
31 ~ 36	I		IOD51~1OD01: Bidirectional I/O data bus
37	I	HLDA	HLDA1: During the CPU cycle, this signal is "1". During the DMA cycle, this signal is "2".
38	O	CALE	CALE1: Address AD191~AD001 is latched at the rising edge of the "H" pulse.
39	O	PDICS	PDICS0: Programmable I/O port chip select signal
40		GND	Ground
41	I	TEST2	PO2A0: Test pin
42	I	WDLEN	WDLEN0: When the word "I/O" is accessed, EVEN data is enabled to be latched.
43	I	WDLAT	WDLAT1: When the word "I/O" is accessed, EVEN data is latched.
44	O	PAGWR	PAGWR0: DMA page register chip select signal
45	O	NMICS	NMICS0: NMI chip select signal
46	O	A00	A001: Address bit 0

Pin	I/O	SYMBOL	Signal name and Description

47	I	BWDIR	BWDIR1: This signal shows the direction of EVEN/ODD data When this signal is "0", it is executed.
48	I	BWHEN	BWHEN0: ODD data enable signal
49	O	MCRCS	MCRCS0: Machine register chip select signal
50	I	IODMS	IODMS0: Memory select signal on the I/O data bus
51	O		SYD61: one of the bidirectiona1 8-bit data bus
52	O	A02	A021: Address bit 2
53		Vcc	+ 5V dc
54		GND	Ground
55	O		SYD71: one of the bidirectional 8-bit data bus
56 ~ 60		A10~06	A101~A061: Adress bit 10 ~ 6
61	I	TEST1	PO2B0: Test pin
62 ~ 64	O	A03~05	A031~A-051: Address bit 3~5
65		GND	Ground
66 ~ 71	O		SYD01~51: Six of the bidirectional data bus
72 73	O	A12, 11	A121, A111: Address bit 12, 11
74	I	MERD	MERD0: Memory read command signal

Pin	I/O	SYMBOL	Signal name and Description
75	O	TIMCS	TIMCS0: Programmable interval timer chip select signal
76	I	INTA	INTA0: Interrupt acknowledge signal
77	O	DMAD7	DMAD71: One of the upper 4 bits of the DMA address input from the 82C37
78		Vcc	+ 5V dc

79		GND	Ground
80 ~ 82	O		DMAD31~01: Three of the upper 4 bits of the DMA address input from the 82C37
83 ~ 86	O		DMAD61~01: Lower 4 bits of the DMA address input from the 82C37. During the CPU cycle, CPU address A041~ A0B1 is output to the 82C37
87	O	DMACS	DMACS0: DMA controller chip select signal
88	I	DALE	DALE1: DMA address IOD71~01 is latched at the leading edge of the "H" pulse.
89	I	AD00	AD001: One of the lower 16 bits of the data bus from the CPU.
90		GND	Ground
91 ~ 100	O	AD01 ~ AD10	AD011~AD101: 10 of the lower 16 bits of the data bus from the CPU, and are bidirectional.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

C.5 1/O DECODER

This is the circuit that decodes the I/O address signals to select the various devices such as 82C59, 82C37, Bus Controller G.A., BIOS ROM, and Back-up RAM, etc..

I/O address of each device above mentioned is as follows;

	I/O address(Hex)	Signal name
82C37	000-01F	DMACS0
82C59	020-03F	INTCS0

82C53	040-05F	TIMCS0
DMA Page Reg.	080-09F	PAGWR0
NMI Mask Reg.	0A0-0BF	NMICS0
PIO	060-07F	PPICS0
Machine Reg.	0E0-0E4	MCRCS0

In the DMA mode, chip select signal should not be output, and therefore, HLDA1 signal must be set to "1" (See C-5 Pin 37).

Each signal is described by the logical mode as follows;

DNACS0 = A9 ù A8 ù A7 ù A6 ù A5 ù HLDA
INTCS0 = A9 ù A8 ù A7 ù A6 ù A5 ù HLDA
TIMCS0 = A9 ù A8 ù A7 ù A6 ù A5 ù HLDA
PAGWR0 = A9 ù A8 ù A7 ù A6 ù A5 ù IOWO ù HLDA
NMICS0 = A9 ù A8 ù A7 ù A6 ù A5 ù IOWO ù HLDA
PPICS0 = A9 ù A8 ù A7 ù A6 ù A5 ù HLDA
MCRCS0 = A9 ù A8 ù A7 ù A6 ù A5 ù A4 ù A3 ù(A2 + A2 ù A1 ù A0) ù HLDA

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

C.6 BACK-UP PORT

Although this system contains the resume function, 82C59 (PIC) and 82C53 (timer) have registers which can not be read, and consequently they can not be backed up for resuming the system. For this reason, when writing the data, the content of these registers must be copied into another readable register, Reading this register can be executed by setting the Index address to the Index register in order to read the data register.

The following table shows the Index address and the contents to be read out.

TABLE C-2 Index Address and Contents

Index Register	Contents to be read in the Port-0FH
50	82C53 Control Word Register, #0
51	" #2
52	82C59 lnitialize Command Word 1

```
ÃÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³        53         ³                "                 2        ³
ÃÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´
³        54         ³                "                 4        ³
ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÁÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

I/O Back-up Index Register 0F0H
I/O Back-up Data Register 0F1H

Both Index register and Data Register are in the "clear" status when power is on.

On writing data, the address of the above 5 registers are as follows;

- CWR#0 (82C53)   043H and moreover, bit 6 and 7 of the write data are "0".

- CWR#2 (82C53)   043H and moreover, bit 6 of the write data is "0", and 7 "1".

- ICW1 (82C59)   020H and moreover, bit 4 of the write data is "1".

- ICW2 (82C59)   021H

- ICW4 (82C59)   021H (data is written after the address ICW2).

FIGURE C-2 Data Register and Index Register

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

D.1 GENERAL

The Display Controller Gate Array is a CMOS type chip with 5,000-gate, 100-pin flat package, and it contains the color graphics adapter which can control both the external CRT display and the internal LCD display.

This gate array contains the following functions.

-LCD/CRT control function
-Attribute process function
-Interface with the CPU (I/O bus)
-Interface with the V-RAM and with the CG-ROM

FIGURE D-1 Display Conroller Gate Array

The detailed description of each pin and signal is also given here.

The whole system including this gate array is called the Display Controller Subsystem, and it can control the following two types of displays.

(A) 640x200 dot LCD (Liquid Cristal Display)
(B) 640x200 dot CRT (Cathode Ray Tube) Display

Note that the external CRT display unit and the internal LCD can not be used at the same time, and its selection is performed by the keyboard operation.

Fn + Home ..... LCD is selected.
Fn + End ..... External CRT display is selected.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

D.2 DISPLAY CONTROLLER SUBSYSTEM (DCS)

FIGURE D-2 Display Controller Subsystem

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU

LANG:TSF
LANG:TISB

D.3 DISPLAY CONTROLLER

Table D-1 Pin Description

Pin	I/O	SYMBOL	Signal name and Description
1	I	CG03	CG31: Character generator output signal bit 3.
2	I	CG04	CG41: Character generator output signal bit 4.
3	I	VCC	+ 5V
4	I	CG05	CG51: Character generator output signal bit 5.
5	I	CG06	CG61: Character generator output signal bit 6.
6	I	CG07	CG71: Character generator output signal bit 7.
7	I	CRMO	CEROM0: Chip enable signal for CG-ROM (Character generator-ROM).
8	I	CG02	CG21: Character generator output signal bit 2.
9	I	CG01	CG11: Character generator output signal bit 1.
10	I	CG00	CG01: Character generator output signal bit 0.
11	O	RS01	RSA01: Raster scan address bit 0.
12	O	RS11	RSA11: Raster scan address bit 1.
13	O	RS21	RSA21: Raster scan address bit 2.
14	O	RS30	RSA31: Raster scan address bit 3. Not used.
15		GND	Ground
16	I	DUTY	DUTY: LCD Duty
17	O	FNS0	INTEN1: Intensified font select signal.(single dot/double dots character)

18	O	FNP0	CGM01: Plasma font selection, (8x8/8x16) This signal is not used in this system.

Pin	I/O	SYMBOL	Description
19	O	CGA1	CGAX1: CG address latch.
20	O	RS0L	RASEL0: Refresh address selection.
21	O	RA12	RA121: Refresh address bit 12.
22	O	RA11	RA111: Refresh address bit 11.
23	O	RA10	RA101: Refresh address bit 10.
24	O	RA09	RA091: Refresh address bit 09.
25	O	RA08	RA081: Refresh address bit 08.
26	O	RA07	RA071: Refresh address bit 07.
27	O	RA06	RA061: Refresh address bit 06.
28	I	VCC	+ 5V
29	O	RA05	RA051: Refresh address bit 05.
30	I	OC14	OSC141: Clock 14.31818 MHz for the video signal
31	I	ISL0	DIOSL0 Display I/O selected. Access signal to the I/O port of the GA.
32	I	MSL0	DMESL0: V-RAM access signal for CPU.
33	I/O	BD07	SYD71: Data bus bit 7.
34	I/O	BD06	SYD61: Data bus bit 6.
35	I/O	BD05	SYD51:

			Data bus bit 5.
36	I/O	BD04	SYD41: Data bus bit 4.

Pin	I/O	SYMBOL	Signal name and Description
37	I/O	BD03	SYD31: Data bus bit 3.
38	I/O	BD02	SYD21: Data bus bit 2.
39	I/O	BD01	SYD11: Data bus bit 1.
40		GND	Ground.
41	I/O	BD00	SYD01: Data bus bit 0.
42	O	RDY	IORDY1: I/O ready signal.
43	I	RST0	RESET0: GA reset signal.
44	I	UA05	A051: CPU address bit 5.
45	I	UA04	A041: CPU address bit 4.
46	I	UA03	A031: CPU address bit 3.
47	I	UA02	A021: CPU address bit 2.
48	I	UA01	A011 CPU address bit 1.
49	I	UA14	A141: CPU address bit 14.
50	I	MEW0	MWR0: Memory write signal.(for V-RAM write)
51	I	MER0	MRD0: Memory read signal. (for V-RAM read)
52	I	IOR0	IORD10: I/O read signal. It read out I/O port data to the data bus BD00-BD07.
53	I	VCC	+ 5V

54	I	IOW0	IOWR10: I/O write signal. It write data on the data bus to the I/O port.

Pin	I/O	SYMBOL	Description
55	I	UA00	A001 CPU address bit 0.
56	I	PDP0	PDP0: Plasma /LCD select.
57	I	GOF1	DGDIS1: GA off. If this signal is high, the GA becomes disabled.
58		TEH1	Ground.
59		TFU1	Ground.
6O		TCN1	Ground.
61	O	N.C.	BFR0: Video signal.
62	O	RHV1	FRHV1: Video signal. Vertical sync. signal for composite CRT display.
63	O	FVS1	FPVS1: Video signal. Vertical sync. signal for LCD/RGB CRT display.
64	O	SXV1	SXVD1: Shift clock for LCD
65	O	GND	Ground.
66	O	LHS1	LPHS1: Video signal. Horizontal sync. signal for LCD/RGB CRT display.
67	O	D0R1	D1R1: Video signal. Red signal for RGB CRT display.
68	O	DIG1	D2G1: Video signal. Green signal for RGB CRT display.
69	O	D2B1	D3B1: Video signal. Blue signal for RGB CRT display.
70	O	D3I1	D4I1: Video signal. Intensity signal for all.
71	I	CHFOT	CHFONT0:

			Change character font signal
72	I	FDIS	FLTDSL1: Flat display selected. It changes internal / external display.

Pin	I/O	SYMBOL	Description
73	I	OC17	OSC171: Clock 17.5 MHz
74	O	CEH0	CEH0: Chip enable high. Chip selected signal for the V-RAM.
75	O	WRC0	WRCC0: Write character code. It is used with chip enable signal to write them to V-RAM. (even address)
76	O	WRA0	WRAT0: Write attribute data. It is used with chip enable signal to write them to V-RAM. (odd address)
77	O	CEL0	CEL0: Chip enable low. It is V-RAM selection signal.
78		VCC	+5V
79	O	RA00	URA001: CPU/Refresh address bit 0.
80	O	RA01	URA011: CPU/Refresh address bit 1.
81	O	RA02	URA021: CPU/Refresh address bit 2.
82	O	RA03	URA031: CPU/Refresh address bit 3.
83	O	RA04	URA041: CPU/Refresh address bit 4.
84	I/O	AT00	AT01: Attribute data bit 0.
85	I/O	AT01	AT11: Attribute data bit 1.
86	I/O	AT02	AT21: Attribute data bit 2:
87	I/O	AT03	AT31L: Attribute data bit 3.

88	I/O	AT04	AT41: Attribute data bit 4.

Pin	I/O	SYMBOL	Signal name and Description
89	I/O	AT05	AT51: Attribute data bit 5.
90	I/O	GND	GROUND
91	I/O	AT06	AT61: Attribute data bit 6.
92	I/O	AT07	AT71: Attribute data bit 7.
93	I/O	CC00	CC01: Character code data bit 0.
94	I/O	CC01	CC11: Character code data bit 1.
95	I/O	CC02	CC21: Character code data bit 2.
96	I/O	CC03	CC31: Character code data bit 3.
97	I/O	CC04	CC41: Character code data bit 4.
98	I/O	CC05	CC51: Character code data bit 5.
99	I/O	CC06	CC61: Character code data bit 6.
100	I/O	CC07	CC71: Character code data bit 7.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU

LANG:TSF
LANG:TISB

D.4 FUNCTIONS OF THE DCS

Display controller subsystem (DCS) is composed of the following components.

TABLE D-2 Components of the Display Controller

Display Controller G A	CMOS 5 KG 100-pin flat Package
Video- RAM	16 K bytes 64 K RAM x 2
CG-ROM	8 K bytes 64 K ROMx1
OSC CPU-CLK	14.31818 MHz
Others Multiplexer Latch Display Buffer	74 HC 157x2 74 HC 273x1

The following table shows the operation modes of the DCS of the internal LCD and external CRT display.

TABLE D-3 LCD/CRT Operation Mode

Operation Mode	LCD/CRT Resolution (Pixels)	LCD/CRT Character Box (Pixels)
40x25TEXT	320x200	8x8
80x25TEXT	640x200	8x8
320x200 GRAPH	320x200	8x8
640x200 GRAPH	640x200	8x8

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU

D.5 VARIOUS SIGNALS

The DCS contains the following different groups of signals;

- I/O Interface signals (23 lines)
- V-RAM signals (34 lines)
- Character Generater (CG) signals (16 lines)
- Video signals (9 lines)
- Display mode selects signals (3 lines)
- Clock input (2 lines)
- Other signals (5 lines)

D.5.1 I/O interface signals

DIOSL0 : Display I/O Select (Input)

When this signal is "0", the CPU is enabled to access the I/O port inside the gate array.
If this signal is "0", either IORD0 or IOWR0 becomes "1", and the CPU is enabled to read or write the I/O port inside the gate array.

IORD0 : I/O Read (Input)

When this signal is low and DIOSL0 is also low, the data of the I/O port is transferred to the CPU through the bus BD00-BD07.

IOWR0 : I/O Write (Input)

When this signal is low and DIOSLO is also low, the data from the CPU is written to the selected 1/0 port inside the gate array through the bus BD00-BD07.

DMESL0 : Display Memory Selected (Input)

When this signal is low, the CPU or DMAC is enabled to access the video RAM. In the same condition, if either MERD0 or MEWR0 is low, read and write operation is enabled.

MERD0 : I/O Read (Input)

When this signal is low and DMESL0 is low, reading operation to V-RAM is executed, and the read data becomes effective in the bus BD00-BD07.

MEWR0 : Memory Write (Input)

When this signal is low and DMESL0 is also low, the data on the bus BD00-BD07 are written to the V-RAM.

UA00-UA05, UA14 (A001-A051,A141) : CPU Address (Input)

These are address data line from the CPU or DMAC, and when it is at high level, it shows logic true.
UA00-UA03 (A0-A3) are used for selecting one of the I/O ports

included in the gate array during read or write operation to the I/O port of the gate array. When memory read or write operation to the V-RAM is performed, memory location is selected by the address lines UA00-UA05 (A0-A5) and also by those of A06-A13 which are supplied directly to the V-RAM without passing the gate array.

BD00-BD07 (SD01-SD71): 8-bit Data Bus (Input/Output)

These are 8-bit data lines and when those signals are at high level, it shows logic true. These lines are used for input or output of the data during read or write operation to the I/O port inside the gate array or to the V-RAM.

IORDY1: I/O Ready (Output)

When access requirement to the V-RAM is generated from the CPU or DMAC, if DMESL0 becomes low, the gate array keeps this signal at low level, and puts the CPU and DMAC in the waiting position until the access is enabled.

RST0 (RESET0): (Reset)

When this signal is at low, the gate array is reset.

D.5.2 V-RAM signals (34 lines)

UR00-UR04: CPU/Refresh Address 00-04 (Input)

RA05-RA12: Refresh Address 05-12 (Input)

These are address lines for the V-RAM.

The 5 address signals UR00-UR04 are directly connected to the address input pin of the V-RAM, while the upper 8 signals on the address lines RA05-RA12 are multiplexed with the address signals A061-A131 of the I/O bus and are connected to the address input pin of the V-RAM.

There are two modes in the accessing the V-RAM; one is the mode in which memory read or write operation from the CPU is executed through the I/O bus, and the other is the one in which the direct display fresh (read only) is performed from the gate array.

CELO, CEHO : Chip Enable Low/High (Output)

These are the chip enable signals for the V-RAM, and at low level the RAM is enabled. Only CELO is used in the system. 2 SRAMs (TC5565), configuration of which is 8k x 8, are used as the RAM.
The RAM connected to the data buses CC00-CC07 are assigned to the even byte, and the one connected to the data buses AT00-AT07 are assigned to the odd byte. 2-byte read operation of display refresh is executed to the V-RAM. When the CPU or the DMAC reads the V-RAM, two bytes of the RAM is enabled, but only one of those two bytes is output to the I/O bus BD00-BD07. This is controlled by UA00 input signal.

When UA00 is at low level, one byte of the CC00-CC07 is output to the bus BD00-BD07, and when UA00 is at high level, one byte of the AT00-AT07 is output to the I/O bus BD00-BD07.
When the CPU or the DMAC writes to the V-RAM, two bytes of the RAM is enabled, but only one of those two RAMs executes the write operation.

WRC0: Write Character Code (Output)

WRA0: Write Attribute Data (Output)

These are the write enable signals to the V-RAM. When the chip enable signal is low and this signal is also low, write operation to the RAM is executed.

Write operation to the RAM is executed only when the request signal from the CPU or the DMAC is generated (when both MSL0 and MEW0 are low). In this case, either WRC0 or WRA0 becomes low depending on the status of UA00. When UA00 is low, WRC0 becomes also low, and write data appears on the CC00-CC07 through the I/O buses BD00-BD07.

When UA00 is high, WRA becomes low, and the write data appears on the AT00-AT07 through BD00-BD07.

Address Assignment of the V-RAM

TABLE D-4 V-RAM Address Assignment

V-RAM Pin Name	V-RAM Signal Name	CPU Address	Memory Refresh TEXT Mode	Memory Refresh GRAPH Mode
CE	CEH0/CEL0	A14	MA13	RSA1
AD12	RA121	A13	MA12	RSA0
AD11	RA111	A12	MA11	MA11
AD10	RA101	A11	MA10	MA10
AD09	RA091	A10	MA09	MA09
AD08	RA081	A09	MA08	MA08
AD07	RA071	A08	MA07	MA07
AD06	RA061	A07	MA06	MA06
AD05	RA051	A06	MA05	MA05
AD04	RA041	A05	MA04	MA04
AD03	RA031	A04	MA03	MA03
AD02	RA021	A03	MA02	MA02
AD01	RA011	A02	MA01	MA01

AD00	RA001	A01	MA00	MA00
WE	WRCC0/ WRAT0	A00	----	----

Note:

- * A00-A14 are address signals from the I/O bus of the CPU.
- * MA00-MA13 are refresh memory address. They are generated by the 6845 circuit or its equivalent inside the gate array.
- * RSA0-RSA1 are raster scan address. They are generated by the 6845 or its equivalent inside the gate array. There are 4 raster scans151together, but only the lowest two bits are used in the graphics mode.

V-RAM Control Signals

FIGURE D-3 V-RAM Control Signals

RASEL0 : Refresh Address Selection (Output)

This signal is an input selection signal to the V-RAM address multiplexer.

If this is low, the display refresh address lines (RA051-RA121) are selected and supplied to the V-RAM. If it is high, the I/O bus address lines are selected and supplied to the V-RAM.

CC01-CC71 : Character Code Data Bus (Input/Output)

These lines are data bus from/to the even address V-RAM. The even address of the V-RAM is used to store the character codes in the TEXT mode.

AT01-AT71 : Attribute Data Bus (Input/Output)

These lines are data bus from/to the odd address V-RAM. The odd address of the V-RAM is used to store the attribute codes in the TEXT mode.

D.5.3 Character generator (CG) signals (16 lines)

CGA1: CG Address Latch (Output)

This signal is used to set the character code read out from the V-RAM in the external latch. The set timing of the external latch circuit is at the raising edge of this signal. The output from the external latch circuit is used for the address of the CG-ROM. As the character code is of 8-bit, it can select one of the 256 characters.

ROM Address : (Output)

The following 6 signals are also used as CG-ROM address apart from the above mentioned character code which are latched in CGA1.

CGM01 .... Plasma Font Selection (Not used)
INTEN1 .... Single Dot Font Selection
RSA01, 11, 21, 31 .... Raster Scan Address

The CG-ROM in this system has the capacity of 8 Kbytes, and it contains the fonts as follows;

8x8 single dot character set
8x8 double dot character set

The LCD can not display intensified character like CRT display, thus double dot character is used for distinction between normal character and intensified character.
INTEN1 signal is used to select either single dot character or double dot character font.

INTEN1 = Low   Single dot character
INTEN1 = high Double dot character

RSA01-RSA21, and RSA31 are raster scan address. The RSA01 is the lowest bit (LSB).

TABLE D-5 ROM Address Assignment

```
ÚÄÄÄÄÄÄÂÄÄÄÄÄÄÂÄÄÄÄÄÄÄÄÂÄÄÄÄÄÄÄÄ¿
³ RSA31³RSA21 ³  RSA11 ³  RSA01 ³
ÃÄÄÄÄÄÄÅÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄ´            ÚÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ¿
³   N  ³  L   ³    L   ³    L   ³-----0  --->³                    ³
³      ÃÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄ´            ³                    ³
³   O  ³  L   ³    L   ³    H   ³-----1  --->³                    ³
³      ÃÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄ´            ³                    ³
³   T  ³  L   ³    H   ³    L   ³-----2  --->³                    ³
³      ÃÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄ´            ³        8x8         ³
³   U  ³  L   ³    H   ³    H   ³-----3  --->³     Character      ³
³      ÃÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄ´            ³                    ³
³   S  ³  H   ³    H   ³    L   ³-----4  --->³                    ³
³      ÃÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄ´            ³                    ³
³   E  ³  H   ³    H   ³    H   ³-----5  --->³                    ³
³      ÃÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄ´            ³                    ³
³   D  ³  H   ³    H   ³    L   ³-----6  --->³                    ³
³      ÃÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄÅÄÄÄÄÄÄÄÄ´            ³                    ³
³      ³  H   ³    H   ³    H   ³-----7  --->³                    ³
ÀÄÄÄÄÄÄÁÄÄÄÄÄÄÁÄÄÄÄÄÄÄÄÁÄÄÄÄÄÄÄÄÙ            ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÙ
```

D.5.4 Video signals (9 lines)

These are 9 video signals output from the gate array, and they are commonly used for the LCD, and for the CRT. Meaning of the signals for each display is as follows;

TABLE D-6 Video Signals

GA signal	LCD	CRT display	
		RGB	Composite
LPHS1	LLP1	CHSY1	-
FPVS1	LFP1	CHSY1	-
FRHV1	LFR1		CMP1
D1R1	LD11	CRV1	CMP1
D2G1	LD21	CGV1	CMP1
D3B1	LD31	CBV1	CMP1
D411	LD41	C1V1	CMP1
SXVD1	LSCK0		CMP1

D.5.5 Display mode select signals (3 lines)

CHFONT0 : Change Character Font (Input)

This signal is to change the font displayed on the screen. The function of this signal is shown on the Table D-7.

FLTDSL1 : Flat Display Selected (Input)

This signal is to select one of internal and external display unit.

If this signal is at high level, the internal LCD is selected.

If this signal is at low level, the external CRT display (RGB, Composite) is selected.

PDP0 (Plasma/LCD Display Panel)

This signal is not used in this system.

When this bit is high, LCD is selected, and normally it is set to high.

The relation of these three signals and character fonts on the screen are as follows;

TABLE D-7 Signals and Character Fonts

	Bit 3 of	GA Input GA output	Selected	Selected

	attribute byte	CHF0 NT0	CHF0 SL1	PDP0	INTE N1	CGM 01	Display Display	Display Display
80x25 or 40x25	0	H	H	H	H	H	LCD	8x8 double
	1	H	H	H	L	H	LCD	8x8 single
	0	L	H	H	L	H	LCD	8x8 single
	1	L	H	H	H	H	LCD	8x8 double
80x25 or 40x25	0	H	L	x	H	H	CRT	8x8 double
	1	H	L	x	H	H	CRT	8x8 double (High)
	0	L	L	x	L	H	CRT	8x8 single
	1	L	L	x	L	H	CRT	8x8 single (High)

D.5.6 Clock input (2 lines)

OSC141: Oscillator 14 MHZ (Input)

This clock is the input signal to generate a video signal for the CRT display.

The frequency of the clock must be 14.31818MHZ.

OSC171 : Oscillator 17.5MHz (Input)

This clock is the input signal to generate a video signal for the plasma display.

The frequency of the clock must be 17.5MHZ.

D.5.7 Other signals (5 lines)

DGDIS1: GA Off (Input)

If this signal is at high level, the gate array is disabled. This signal is used to disable the gate array in order to connect another display adapter to the I/O expansion box. In this system, this is fixed to NON.

DUTY: DUTY-LCD (Input)

This is SCAN DUTY select signal for the LCD display. When this bit is "1", 1/200 duty is selected, and when NON, 1/100 duty is selected.

In this system, this bit is always set to "1".

E.1 GENERAL

This gate array is compatible with Lotus/Intel/Microsoft Expanded Memory Specification, and is composed of 100 pins altogether.

Within the memory address space C4000H-EFFFFH, the consecutive 64-kbyte space is reserved as the EM window.

Each EM unit can control up to 2 Mbytes (128 pages), and as one system can control up to four EM units, the whole system can have maximum 8-Mbyte space.
All of this is possible in theory, but in fact, as there is a limit in the real installation, the maximum 384-kbyte address space is provided as its standard mode.

I/O ports used for the EM unit are 2X8H-2XFH, and different I/O port is assigned for each unit (X can be any of the numbers - 0, 1, 5, 6, A, B, E).
Through the Page Register in the EM assigned to this I/O port, 64-kbyte window can be assigned on the Expansion Memory.

E-2 MEMORY ASSIGNMENT FOR THE EM UNIT

FIGURE E-1 MEMORY ASSIGNMENT FOR THE EMU

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

E.3 PIN DESCRIPTION

TABLE E-1 Pin Description

Pin	I/O	SYMBOL	Signal name and Description
1	O	RAS1H	RAS1H0: Memory RAS timing signal
2	O	RAS1L	RAS1L0: Memory RAS timing signal
3	I	Vcc	MVRAM: 5Vdc
4	O	RAS0H	RAS0H0: Memory RAS timing signal
5	O	RAS0L	RAS0L0: Memory RAS timing signal
6	O	CAS	CAS0: Memory CAS timing signal
7	O		DRA81: Memory ROW/COL address
8 ~ 14	O		DRA71 ~ DRA11: Memory ROW/COL address
15		GND	Ground
16	O		DRA01: Memory Row/COL address
17	O	IRQ4	IRQ41; Interrupt request 4
18	O	IRQ3	IRQ31: Interrupt request 3
19	O		CMCK1(DACK00): Communication Clock/refresh (Expansion Interface)
20	O		MDSL0/IRQ41: When the modem card is used, modem select signal, and when I/F, interrupt request 4

21	I	SPTON	SPTON0: Speaker drive signal
22	O	BRDIS	BRDIS1: Back-up RAM disable signal
23	O	BMDSL	BMDSL0: Built-in modem select signal
24	O	BMPOF	BMPOF0: Built-in modem power off signal
25	O	HDDSL	HDDSL0: HDD select
26	O	PNLOF	PNLOF0: Panel close signal
27	O	OUT2	OUT21: RS232C interrupt mask

Pin	I/O	SYMBOL	Signal name and Description
28	I	Vcc	MVRAM: 5Vdc
29	I	COMCLK	COMCLK1: Communication clock
30	I	C32KH	C32KH1: PTC clock
31	I	CPCLK	CPCLK1: CPU clock signal
32	I	AEN	DMAEN1: DMA address enable
33	I	DMCLK	DMCLK1: CPU clock signal
34	O	EXMSL	EXMSL0: Expasded memory select
35	O	INTPS	PSNMI1: PS NMI signal
36	I	RASTH	RASTH0: RAS timing high (A00 = ODD)
37	I	RASTL	RASTL0: RAS timing low (A00 = EVEN)
38	I	SPKDR	SPKDR0: Speaker drive signal
39	I	RFSTR	RFSTR1: Refresh start signal
40		GND	Ground
41	O	SPK	SPK1: Speaker on signal
42	O	R232C5	R232CS0: RS232C select
43	O	RTCCS	RTCCS0: RTC select
44	O	RTCRD	RTCRD0: RTC real command
45	O	RTCWR	RTCW0: RTC write command
46	I	BMIRQ	BMIRQ0: Built-in modem interrupt request
47		TEST2	Not used

48		TEST1	Not used
49	I	INT	INT0: RS232C interrupt
50	I	BMSPK	BMSPK0: Built-in modem speaker drive

Pin	I/O	SYMBOL	Signal name and Description
51	I	RFEND	RFEND1: Refresh end signal
52	I	FDRDY	FDRDY1: FDD ready
53	I	Vcc	MVRAM: 5Vdc
54	I	LBAT	LBAT0: Low battery signal
55	O		A011: System address bus
56	I	RPDA	RPDAT1: Receive PS data
57	I	ZRDIS	ZRDIS0: V-RAM disable signal
58	I	MIRQ	MIRQ0: Modem interrupt request
59	O	SPDA	SPDAT0: Send PS data. Normally inverted data is output
60	O	PRTSL	PRTSL0: Printer select signal
61	I	CEL	CEL0: V-RAM chip enable signal
62	I	A00	AOB1: System address
63	I	DACK0	DACK0: Memory refresh signal
64	O	FDDSL	FDDSL0: FDD select signal
65		GND	Ground
66	O	DGDIS	DGDIS1: Display GA disable
67	I	IOR	IORD0: I/O read. When this is low, data is output
68	I	IOW	IOWR0: I/O write
69	I	RESET	RESET0: System address bus
70 ~ 74	I	A19~15	A191 ~ 151: System address bus
75	I	A13	A131: System address bus

76	I	A02	A021: System address bus
77	I	A14	A141: System address bus

Pin	I/O	SYMBOL	Signal name and Description
78	I	Vcc	MVRAM: SVdc
79	I	A03	A031: System address bus
80	I	A04	A041: System address bus
81	O	DIOSL	DIOSL0: Display select signal
82 ~ 88	I	A06 ~ A12	A061: System address bus
89	I	D0	SYD01: System address bus
90		GND	Ground
91 ~ 97	I	D1~D7	5YD11~SYD71: System address bus
98	O	RAS2H	RAS2H0: Memory RAS timing
99	O	RAS2L	RAS2L0: Memory RAS timing
100	I	A05	A0S1: System address bus

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

E.4 CONFIGURATION PORT OF THE EM UNIT

An EM board currently sold on the market has a configuration

switch for I/O address setting.
In the T1200 system, configuration of the EM unit is executed by setting the ports 0EEH and 0EFH as the index register and data register for each.

Definition of these two registers are as follows;

TABLE E-2 Index/Data Registers and Bit Assignment
of the EMC Register

	Index Address	Data Register	
		Write	Read
	50	EM Conf. Reg. - 0	

		Write	Read
EM	bit-7	-	EMU ID bit -3
Conf.	-6	-	" -2
Reg.-0	-5	-	" -1
	-4	-	" -0
	-3	EMU Port bit-3	<--
	-2	" -2	<--
	-1	" -1	<--
	-0	" -0	<--
EM	bit-7		Block SEL 2
Conf.	-6		Block SEL 1
Reg.-1	-5		Block SEL 0
	-4	Hard RAM bit-4	<--
	-3	" -3	<--
	-2	" -2	<--
	-1	" -1	<--
	-0	" -0	<--

Note: Configuration registers 1 and 2 are both reset
to "0" when power is on.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

<fig id=MMS\1200\1200E_8.TIF>Page E-8

E.5 INDEX REGISTER (PORT 0EEH).....WRITE ONLY

In the standard EM unit, index address 50 and 51 are used in its index register.
After using the index address, BIOS always clears to "0", so that content of the data register should not be changed by any other program except BIOS.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB
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E.6 EM CONFIGURATION REGISTER- 0 (INDEX 50/60)

E.6.1

Within this register, I/O address of the EM unit is set by the bits 3--0 of the EMU port, while bits 7--4 are not used.

Bit				I/O Address
3	2	1	0	(When Power is on)
0	0	0	0	208H ~ 20FH
0	0	0	1	218H ~ 21FH
0	1	0	1	258H ~ 25FH
0	1	1	0	268H ~ 26FH
1	0	1	0	2A8H ~ 2AFH
1	0	1	1	2B8H ~ 2BFH
1	1	1	0	2E8H ~ 2EFH
X	1	1	1	Disable*

Note: *Disable = Read/Write operation towards the expansion memory is disabled.

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E.6.2

Bits 7-4 of this register shows the ID bits 3-0 of the EM unit, and these ID codes are used to keep the compatibility with the up-revisioned EMU in the future. The ID of the current EM unit is 8H. By bits 3-0 of this register, I/O port address set on writing is read.

MODEL:T1200F/FB

LANG:TAIS
LANG:No Price
LANG:TAP
LANG:TEG
LANG:TEG uni
LANG:GER ASP
LANG:TEG Dealer
LANG:TIU
LANG:TSF
LANG:TISB

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E.7 EM CONFIGURATION REGISTER - 1 (INDEX 51/61)

E.7.1

Bits 7-6 (Not used)

Bit 5 (Not used)

Bits 4-0 ..... Hard RAM bits 4-0

These are the bits used when expansion memory is used as the Hard RAM.
The expansion memory with the following capacity is used as the Hard RAM.

Bit					Real memory capacity of the EM
4	3	2	1	0	
0	0	0	0	0	0
0	0	0	0	1	64 kbytes (4 pages)
0	0	0	1	0	128 kbytes (8 pages)
??	??	??	??	??	???
1	1	1	1	1	2 Mbytes (128 pages)

These bits 4-0 are not used as hardware of the EM, but as software (RMM, SYS, BIOS). From the hardware's point of view, it can be seen as if simply Read/Write possible register exists.

E.7.2 <Read>

The contents written in the register can be read out.

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TABLE E-3 Memory Address Block

BLK NO.	BSL 2	BSL 1	BSL 0	PAGE ENABLE 0	PAGE ENABLE 1	PAGE ENABLE 2	PAGE ENABLE 3
0	0	0	0	`D0000' ~ `D3FFF'	`C4000' ~ `C7FFF'	`C8000' ~ `CBFFF'	`CC000' ~ `CFFFF'
1	0	0	1	`D0000' ~ `D3FFF'	`D4000' ~ `D7FFF'	`C8000~ ~ `CBFFF'	`CC000' ~ `CFFFF'
2	0	1	0	`D0000' ~ `D3FFF'	`D4000' ~ `D7FFF'	`D8000' ~ `DBFFF'	`CC000' ~ `CFFFF'
3	0	1	1	`D0000' ~ `D3FFF'	`D4000' ~ `D7FFF'	`D8000' ~ `DBFFF'	`DC000' ~ `DFFFF'
4	1	0	0	`E0000' ~ `E3FFF'	`D4000' ~ `D7FFF'	`D8000' ~ `DBFFF'	`DC000' ~ `DFFFF'
5	1	0	1	`E0000' ~ `E3FFF'	`E4000' ~ `E7FFF'	`D8000' ~ `DBFFF'	`DC000' ~ `DFFFF'

```
³ 6 ³ 1³ 1 ³0 ³ `E0000'      ³  `E4000'     ³   `E8000'    ³     `DC000'
³
³   ³  ³   ³  ³ ~ `E3FFF'     ³  ~ `E7FFF'   ³   ~ `EBFFF' ³     ~
`DFFFF' ³
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ÄÄ´
³ 7 ³ 1³ 1 ³1 ³ `E0000'      ³  `E4000'     ³   `E8000'    ³     `EC000'
³
³   ³  ³   ³  ³ ~ `E3FFF'     ³  ~ `E7FFF'   ³   ~ `EBFFF' ³     ~
`EFFFF' ³
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